



SHENZHEN TUOFENG SEMICONDUCTOR TECHNOLOGY CO.,LTD

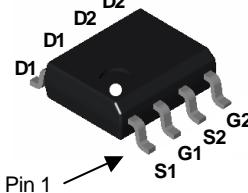
SOP-8L Dual 20V P-Channel PowerTrench[®] MOSFET

TF4953B

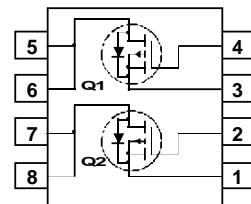
TF4953B Dual P-Channel 20-V(D-S) MOSFET

V_{(BR)DSS}	R_{D(on)MAX}	I_D
-20V	0.075Ω@-4.5V	-5.0A
	0.110Ω@-2.5V	

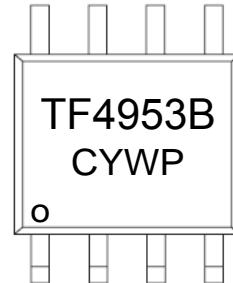
SO-8L



Equivalent Circuit



MARKING



Y :year code W :week code

APPLICATION

- Load Switch for Portable Devices
- DC/DC Converter

Maximum ratings (T_a=25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V _{DS}	-20	V
Gate-Source Voltage	V _{GS}	±12	
Continuous Drain Current	I _D	-5.0	A
Pulsed Drain Current	I _{DM}	-10	
Continuous Source-Drain Diode Current	I _S	-1.30	
Maximum Power Dissipation	P _D	1.0	W
Thermal Resistance from Junction to Ambient(t ≤5s)	R _{θJA}	125	°C/W
Junction Temperature	T _J	150	°C
Storage Temperature	T _{stg}	-55 ~+150	



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SOP-8L Dual 20V P-Channel PowerTrench[®] MOSFET

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Electrical Characteristics

 $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	$V_{\text{GS}} = 0 \text{ V}$, $I_D = -250 \mu\text{A}$	-20			V
$I_{\text{DS}(\text{SS})}$	Zero Gate Voltage Drain Current	$V_{\text{DS}} = -16 \text{ V}$, $V_{\text{GS}} = 0 \text{ V}$		-1		μA
I_{GSSF}	Gate–Body Leakage, Forward	$V_{\text{GS}} = -10 \text{ V}$, $V_{\text{DS}} = 0 \text{ V}$		-100		nA
I_{GSSR}	Gate–Body Leakage, Reverse	$V_{\text{GS}} = 10 \text{ V}$, $V_{\text{DS}} = 0 \text{ V}$		100		nA
On Characteristics						
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	$V_{\text{DS}} = V_{\text{GS}}$, $I_D = -250 \mu\text{A}$	-0.5	-0.7	-1.0	V
$R_{\text{DS}(\text{on})}$	Static Drain–Source On–Resistance	$V_{\text{GS}} = -2.5 \text{ V}$, $I_D = -2.5 \text{ A}$		88	110	$\text{m}\Omega$
		$V_{\text{GS}} = -4.5 \text{ V}$, $I_D = -3.5 \text{ A}$		60	75	
$I_{\text{D}(\text{on})}$	On–State Drain Current	$V_{\text{GS}} = -4.5 \text{ V}$, $V_{\text{DS}} = -4.5 \text{ V}$	-10			A
g_{FS}	Forward Transconductance	$V_{\text{DS}} = -5 \text{ V}$, $I_D = -2 \text{ A}$		5		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{\text{DS}} = -10 \text{ V}$, $V_{\text{GS}} = 0 \text{ V}$, $f = 1.0 \text{ MHz}$		405		pF
C_{oss}	Output Capacitance			75		pF
C_{rss}	Reverse Transfer Capacitance			55		pF
Switching Characteristics						
$t_{\text{d}(\text{on})}$	Turn–On Delay Time	$V_{\text{DD}} = -10 \text{ V}$, $I_D = -1 \text{ A}$, $V_{\text{GS}} = -4.5 \text{ V}$, $R_{\text{GEN}} = 10\Omega$		11		ns
t_r	Turn–On Rise Time			35		ns
$t_{\text{d}(\text{off})}$	Turn–Off Delay Time			30		ns
t_f	Turn–Off Fall Time			10		ns
Q_g	Total Gate Charge	$V_{\text{DS}} = -10 \text{ V}$, $I_D = -3 \text{ A}$, $V_{\text{GS}} = -2.5 \text{ V}$		3.3	12	nC
Q_{gs}	Gate–Source Charge			0.7		nC
Q_{gd}	Gate–Drain Charge			1.3		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I_s	Maximum Continuous Drain–Source Diode Forward Current			-1.3		A
V_{SD}	Drain–Source Diode Forward Voltage	$V_{\text{GS}} = 0 \text{ V}$, $I_s = -1.3 \text{ A}$		-0.8	-1.2	V

Notes:

- R_{\thetaJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{\thetaJC} is guaranteed by design while R_{\thetaCA} is determined by the user's board design.

Typical Electrical and Thermal Characteristics

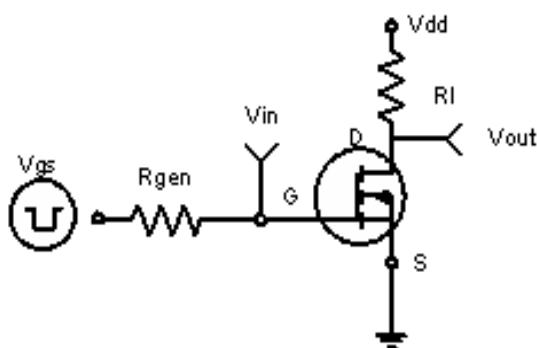


Figure 1:Switching Test Circuit

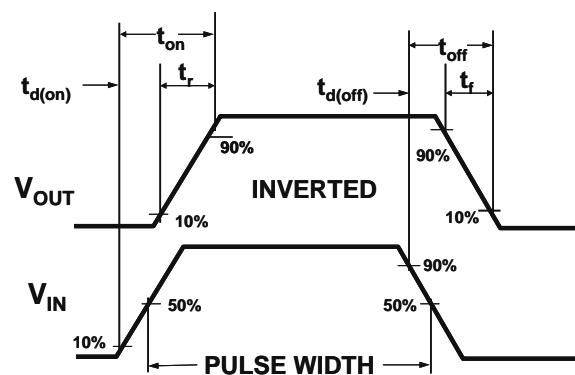


Figure 2:Switching Waveforms

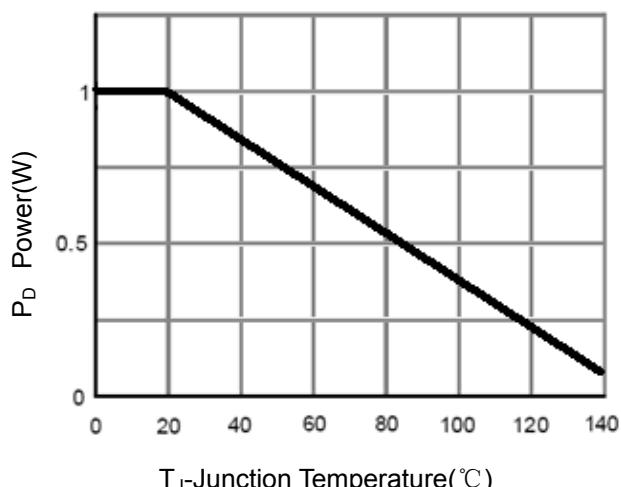
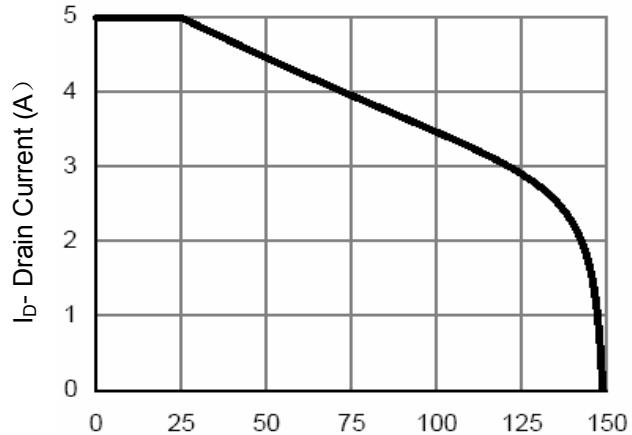


Figure 3 Power Dissipation



T_J-Junction Temperature(°C)

Figure 4 Drain Current

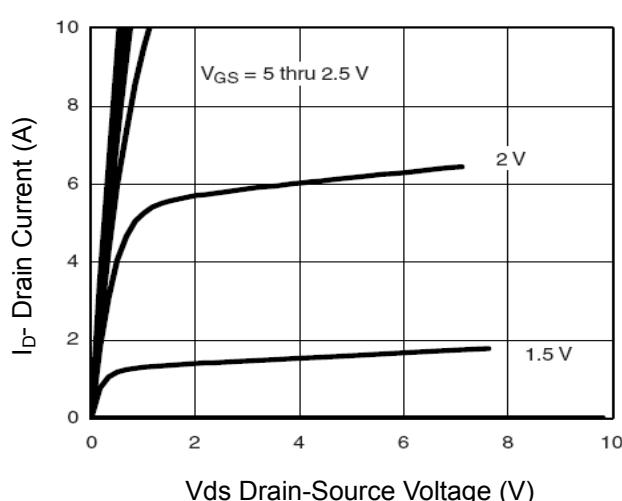


Figure 5 Output Characteristics

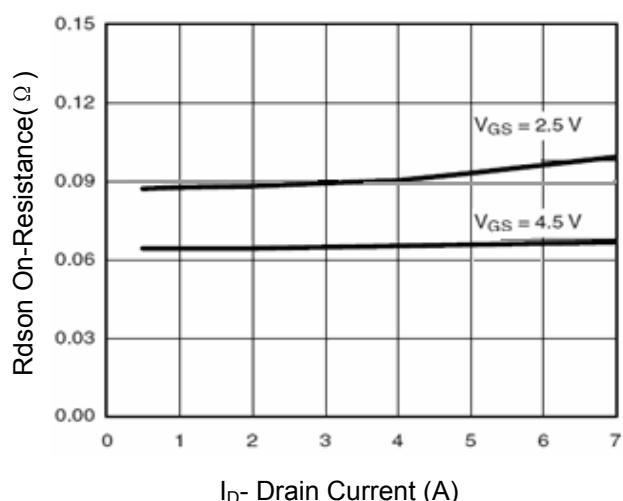


Figure 6 Drain-Source On-Resistance

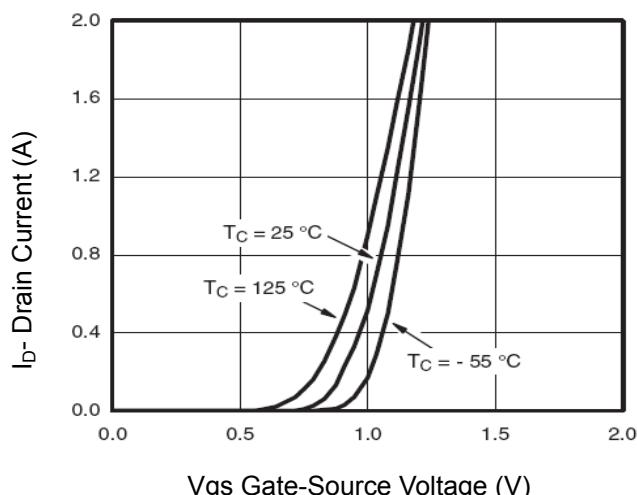


Figure 7 Transfer Characteristics

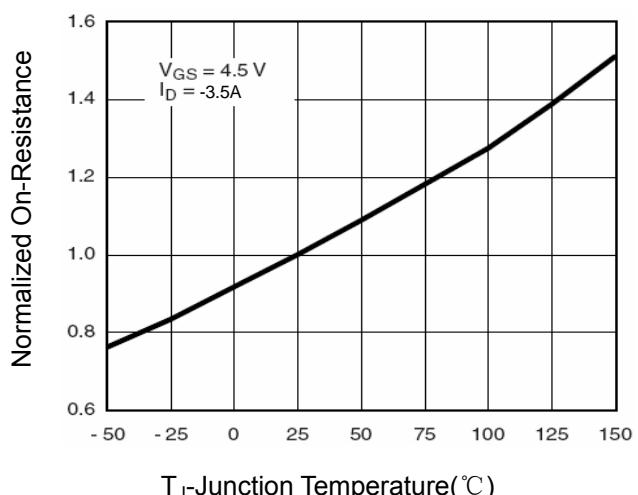


Figure 8 Drain-Source On-Resistance

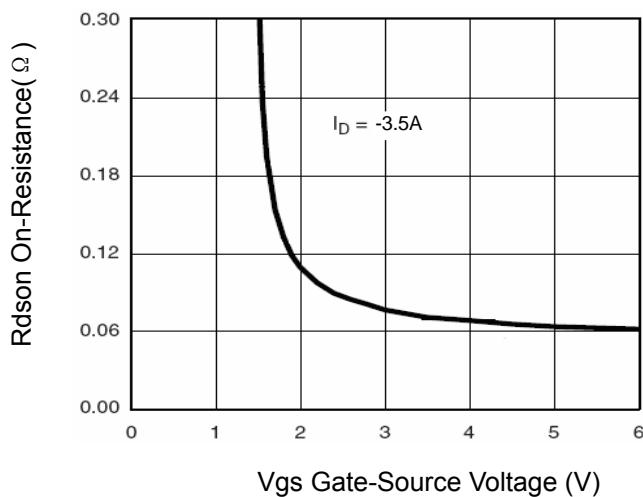


Figure 9 Rdson vs Vgs

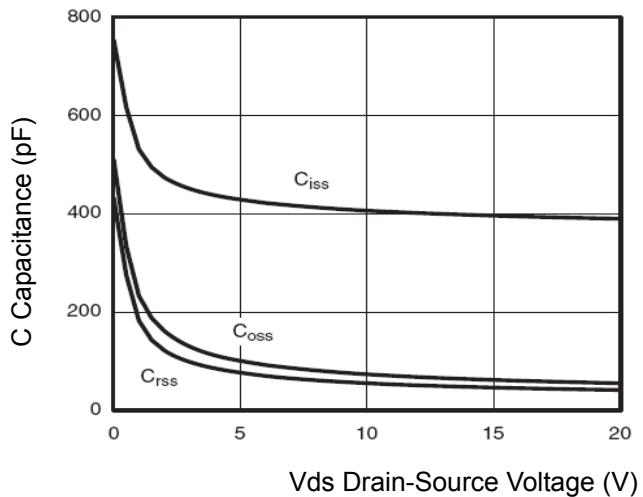


Figure 10 Capacitance vs Vds

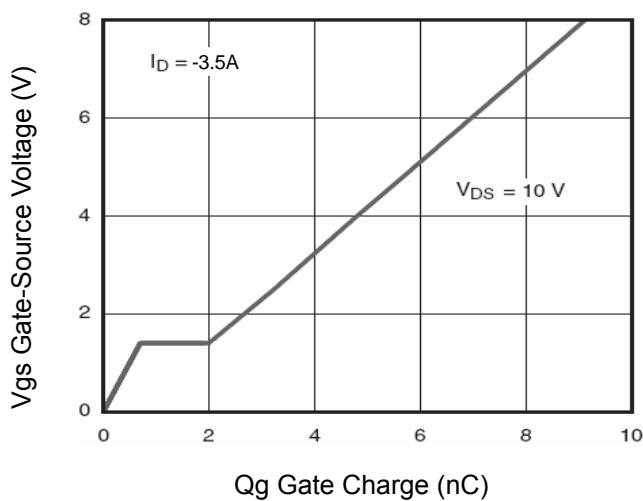


Figure 11 Gate Charge

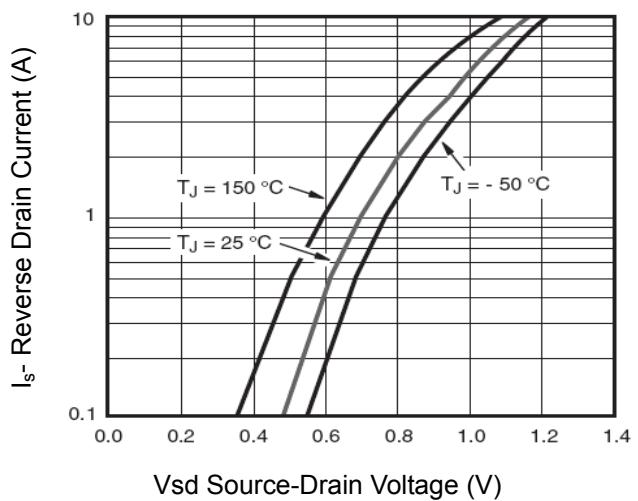
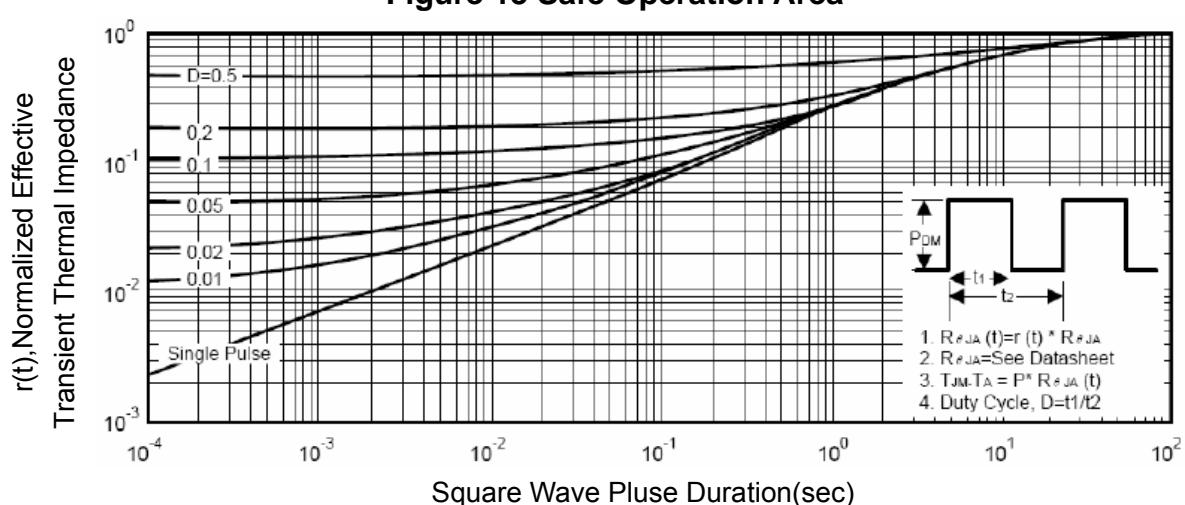
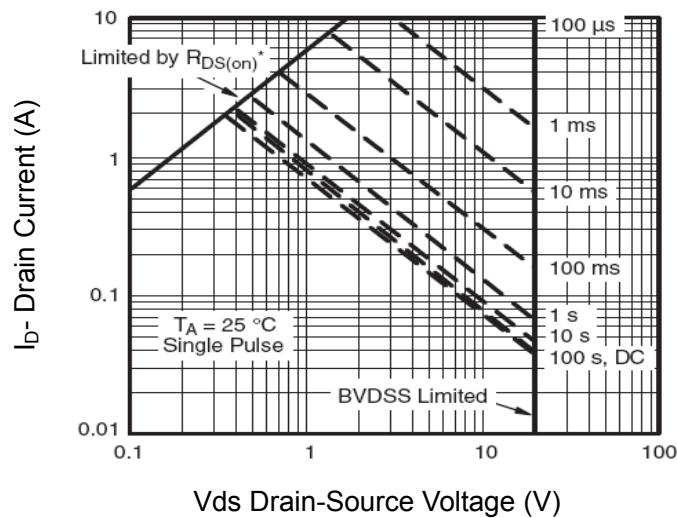
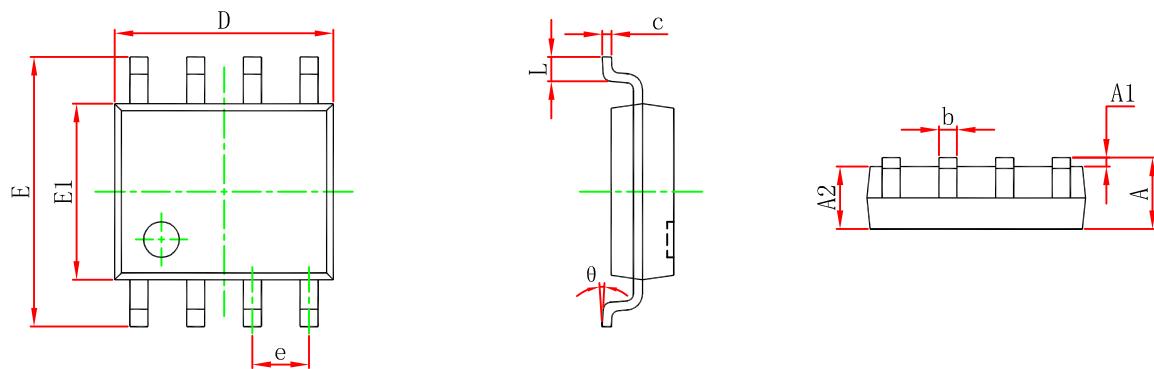


Figure 12 Source- Drain Diode Forward

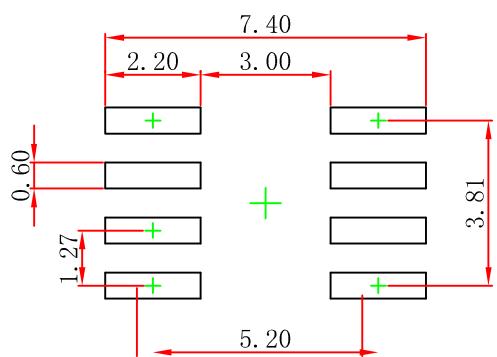


SOP8 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

SOP8 Suggested Pad Layout



Note:
 1. Controlling dimension:in millimeters.
 2. General tolerance: $\pm 0.05\text{mm}$.
 3. The pad layout is for reference purposes only.