

P-Channel Enhancement Mode Power MOSFET

Description

The TF4803A uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge . The complementary MOSFETs may be used to form a level shifted high side switch, and for a host of other applications.

General Features

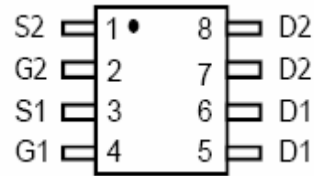
$V_{DS} = -30V, I_D = -6.0A$

$R_{DS(ON)} < 25m\Omega @ V_{GS} = -10V$

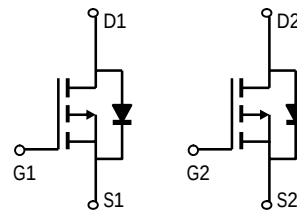
$R_{DS(ON)} < 29m\Omega @ V_{GS} = -4.5V$

- High power and current handling capability
- Lead free product is acquired
- Surface mount package

SOP-8



Equivalent Circuit



MARKING



Y :year code W :week code

Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^A	I_D	-6	A
Pulsed Drain Current ^B	I_{DM}	-20	A
Power Dissipation ^A	$T_A=25^\circ C$	2	W
	$T_A=70^\circ C$	1.4	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ C$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	48	62.5	$^\circ C/W$
Maximum Junction-to-Ambient ^A		74	110	$^\circ C/W$
Maximum Junction-to-Lead ^C	$R_{\theta JL}$	35	40	$^\circ C/W$

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Electrical Characteristics (T_j=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =-250μA, V _{GS} =0V	-30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-24V, V _{GS} =0V			-100	nA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250μA	-1.1	-1.4	-2.1	V
I _{D(ON)}	On state drain current	V _{GS} =-4.5V, V _{DS} =-5V	-20			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =-10V, I _D =-5.5A		25	30	mΩ
		V _{GS} =-4.5V, I _D =-4.5A		29	40	mΩ
g _{FS}	Forward Transconductance	V _{DS} =-5V, I _D =-5A	6	8.6		S
V _{SD}	Diode Forward Voltage	I _S =-1A, V _{GS} =0V		-0.8	-1	V
I _S	Maximum Body-Diode Continuous Current				-2.3A	

DYNAMIC PARAMETERS

C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =-15V, f=1MHz		700		pF
C _{oss}	Output Capacitance			120		pF
C _{rss}	Reverse Transfer Capacitance			75		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		10		Ω

SWITCHING PARAMETERS

Q _g (10V)	Total Gate Charge (10V)	V _{GS} =-10V, V _{DS} =-15V, I _D =-5A		14.7		nC
Q _g (4.5V)	Total Gate Charge (4.5V)			7.6		nC
Q _{gs}	Gate Source Charge			2		nC
Q _{gd}	Gate Drain Charge			3.8		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =-10V, V _{DS} =-15V, R _L =3Ω, R _{GEN} =3Ω		8.3		ns
t _r	Turn-On Rise Time			5		ns
t _{D(off)}	Turn-Off DelayTime			29		ns
t _f	Turn-Off Fall Time			14		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =-5A, dI/dt=100A/μs		23.5		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =-5A, dI/dt=100A/μs		13.4		nC

A: The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design. The current rating is based on the t_s ≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C: The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

D: The static characteristics in Figures 1 to 6,12,14 are obtained using 80μs pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

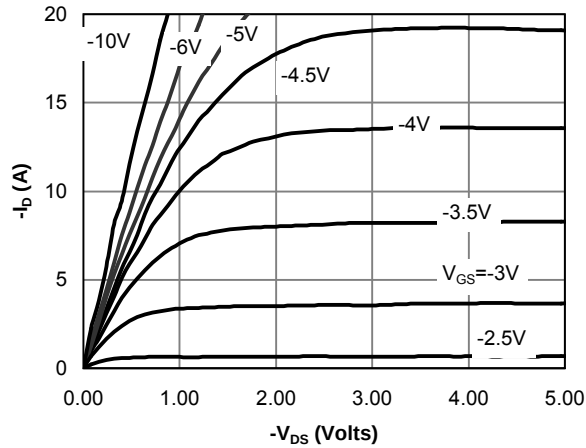


Figure 1: On-Region Characteristics

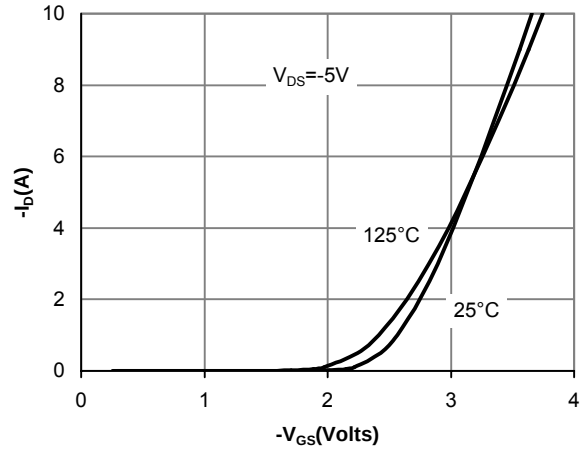


Figure 2: Transfer Characteristics

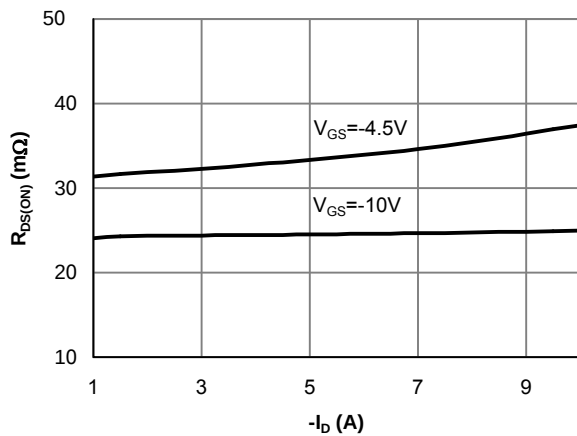


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

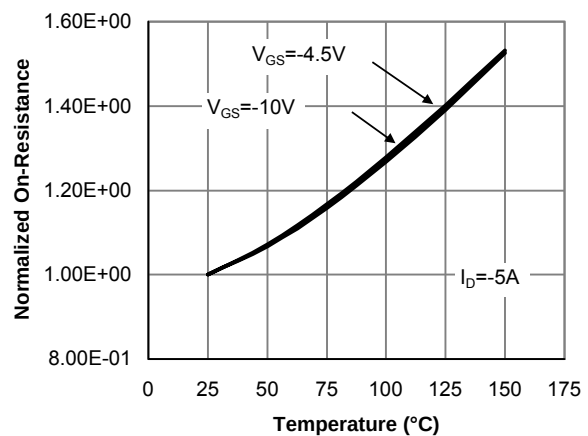


Figure 4: On-Resistance vs. Junction Temperature

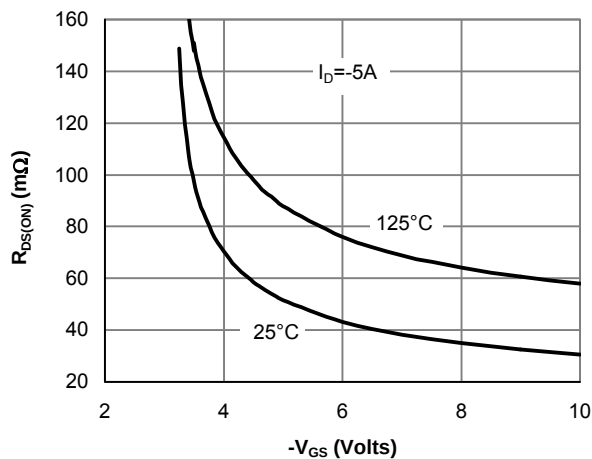


Figure 5: On-Resistance vs. Gate-Source Voltage

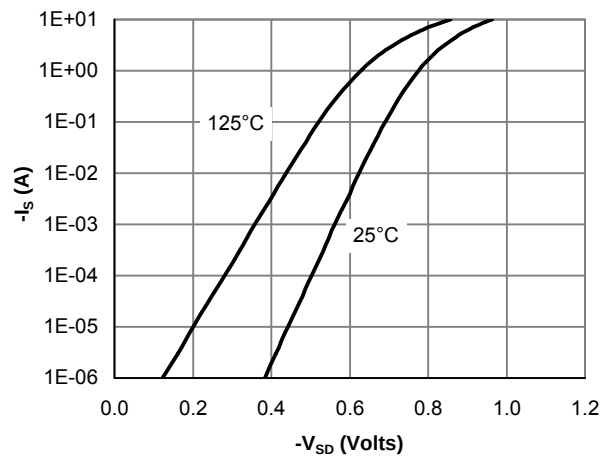


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

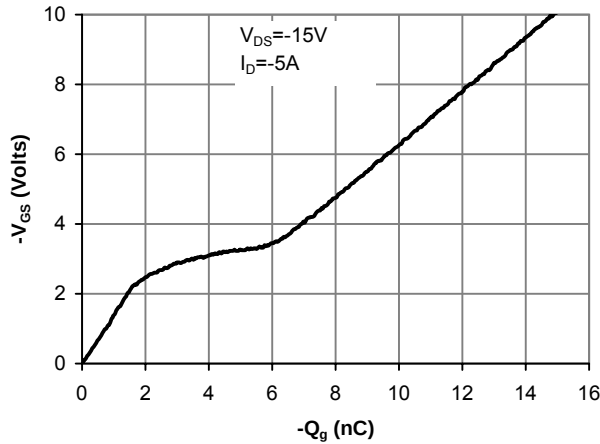


Figure 7: Gate-Charge Characteristics

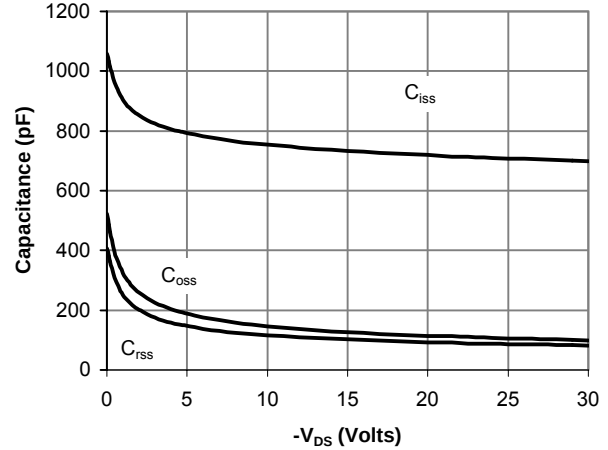


Figure 8: Capacitance Characteristics

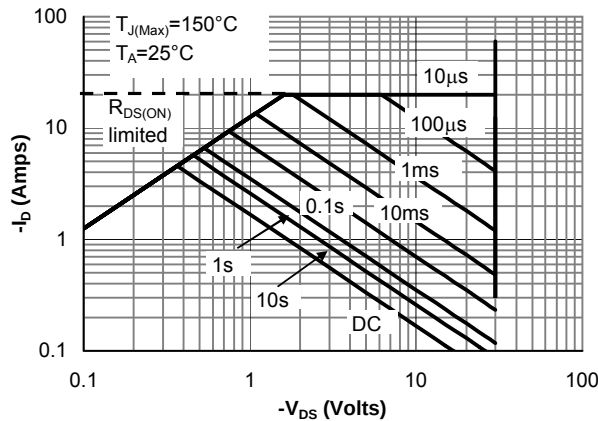


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

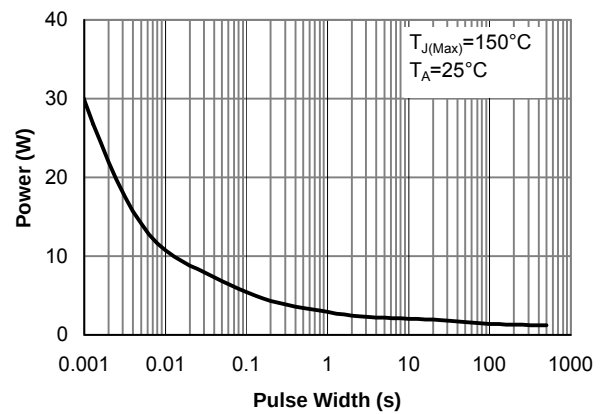


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

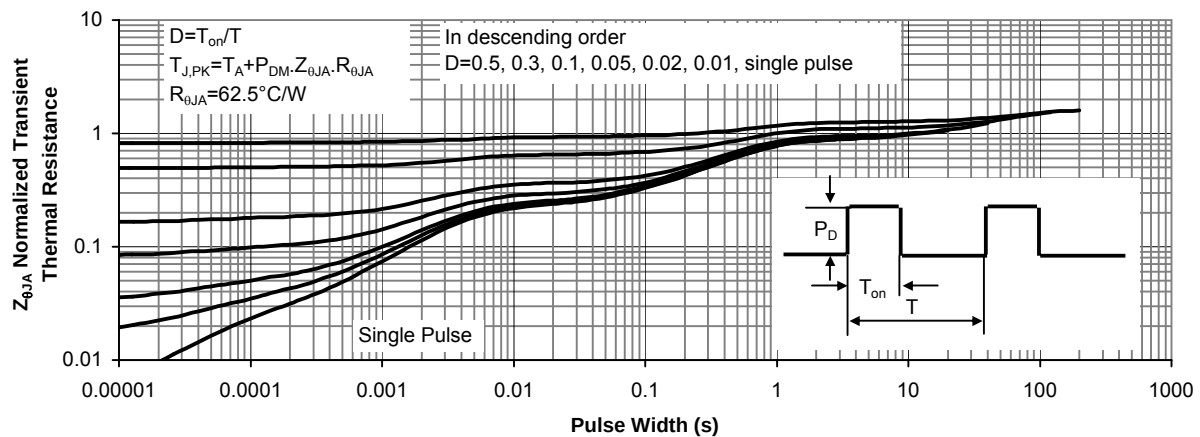
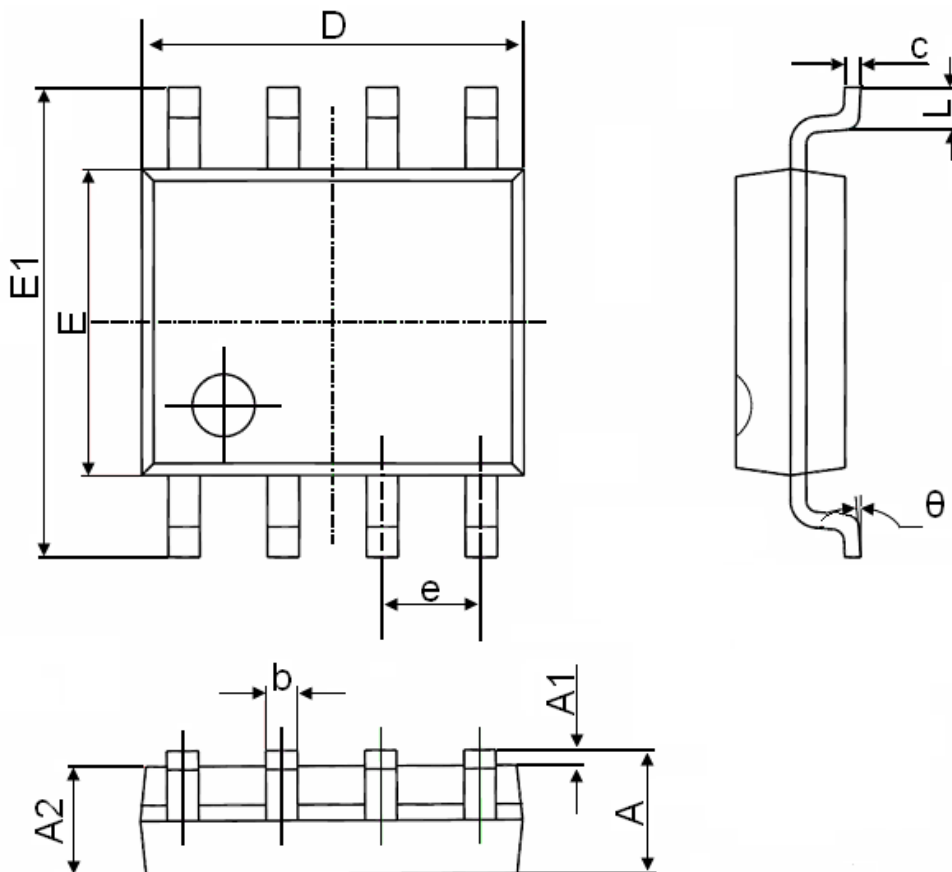


Figure 11: Normalized Maximum Transient Thermal Impedance

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TF4803A

SOP-8 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°