

• General Description

The TFD130N04S combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. This device is ideal for load switch and battery protection applications.

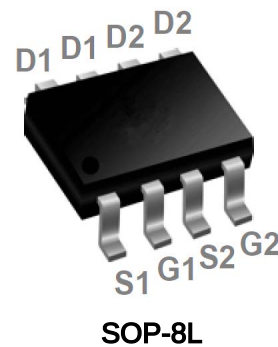
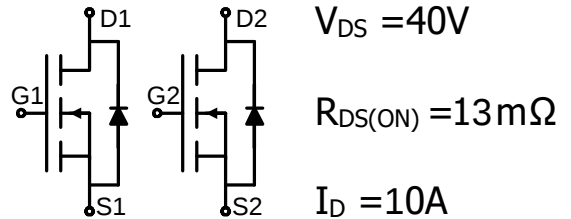
• Features

- Advance high cell density Trench technology
- Low $R_{DS(ON)}$ to minimize conductive loss
- Low Gate Charge for fast switching
- Dual DIE in one package

• Application

- Power Management in Notebook Computer,
- Portable Equipment and Battery
- Powered Systems

• Product Summary



• Package Marking and Ordering Information:

Part NO.	TFD130N04S
Marking	D130N04S
Packing Information	---
Basic ordering unit (pcs)	4000

• Absolute Maximum Ratings ($T_C = 25^\circ\text{C}$)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	$I_{D@TC=25^\circ\text{C}}$	10	A
	$I_{D@TC=75^\circ\text{C}}$	8.0	A
	$I_{D@TC=100^\circ\text{C}}$	6.0	A
Pulsed Drain Current ①	I_{DM}	30	A
Total Power Dissipation	$P_{D@TC=25^\circ\text{C}}$	3.6	W
Total Power Dissipation	$P_{D@TA=25^\circ\text{C}}$	1.5	W
Operating Junction Temperature	T_J	-55 to 150	$^\circ\text{C}$
Storage Temperature	T_{STG}	-55 to 150	$^\circ\text{C}$
Single Pulse Avalanche Energy	E_{AS}	40	mJ

●Thermal resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance, junction - case	R_{thJC}	-	-	2.5	° C/W
Thermal resistance, junction - ambient	R_{thJA}	-	-	75	° C/W
Soldering temperature, wavesoldering for 8 s	T_{sold}	-	-	265	° C

●Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	40	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	1.2	1.5	2.5	V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=40V, V_{GS}=0V$	-	-	1.0	μA
Gate- Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
Static Drain-source On Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=10A$	-	13	18	m Ω
		$V_{GS}=4.5V, I_D=6A$	-	16	20	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=25V, I_D=10A$	-	8	-	S
Source-drain voltage	V_{SD}	$I_S=10A$	-	-	1.20	V

●Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Input capacitance	C_{iss}	f = 1MHz $V_{DS}=20V$ $V_{GS}=0V$	-	1137	-	pF
Output capacitance	C_{oss}		-	84	-	
Reverse transfer capacitance	C_{rss}		-	72	-	

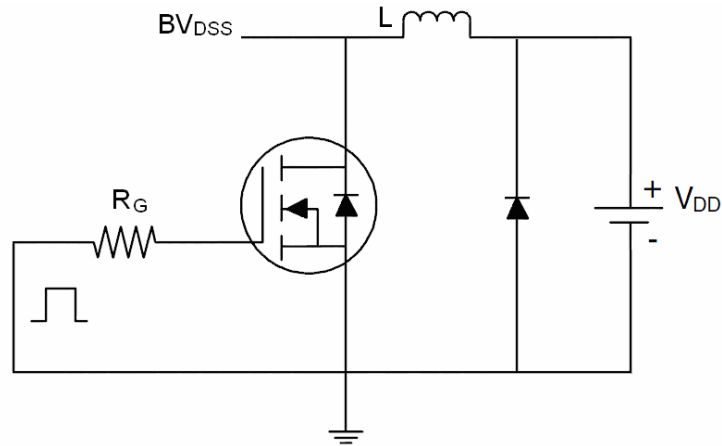
●Gate Charge characteristics($T_a = 25^\circ C$)

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Total gate charge	Q_g	$V_{DD}=20V$	-	25	-	nC
Gate - Source charge	Q_{gs}	$I_D=8A$	-	3.6	-	
Gate - Drain charge	Q_{gd}	$V_{GS}=10V$	-	4.4	-	

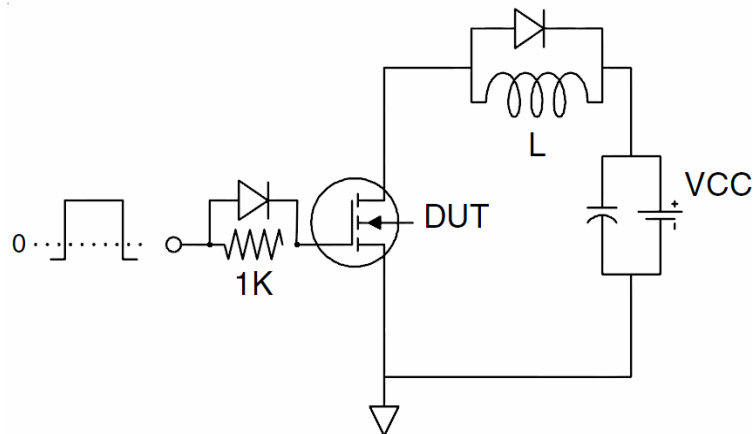
Note: ① Pulse Test : Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$;

Test Circuit

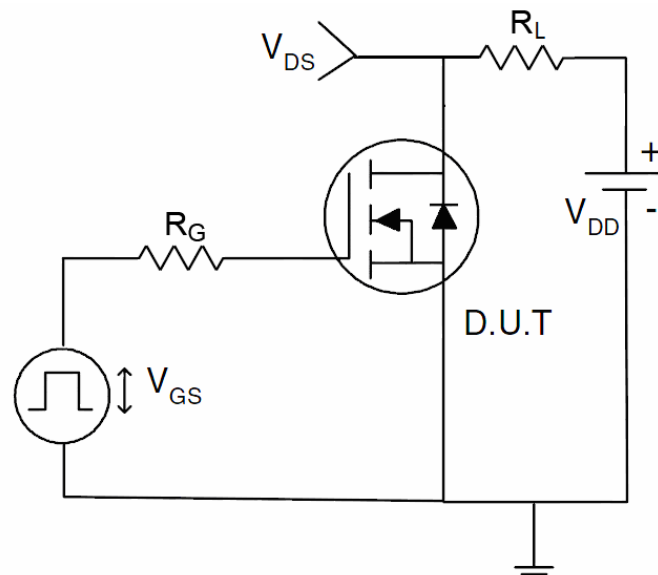
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics

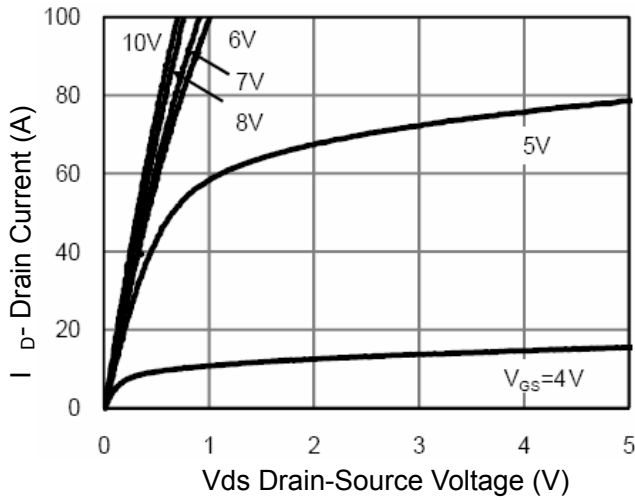


Figure 1 Output Characteristics

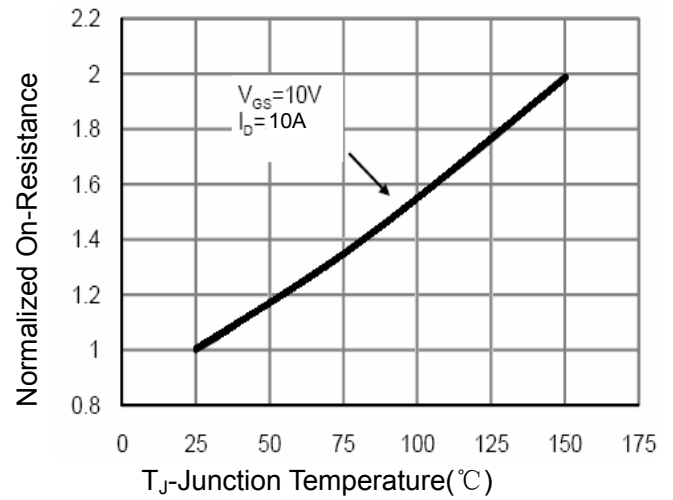


Figure 4 $R_{DS(on)}$ -Junction Temperature

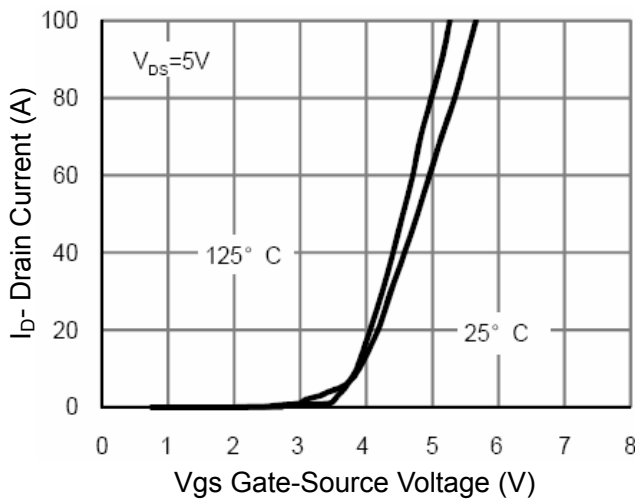


Figure 2 Transfer Characteristics

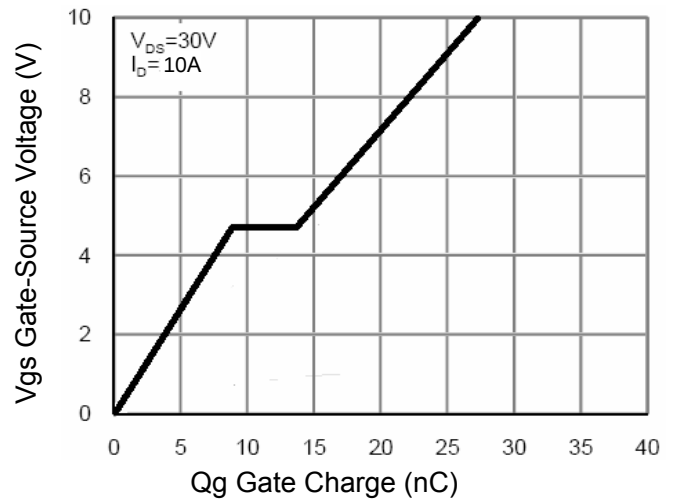


Figure 5 Gate Charge

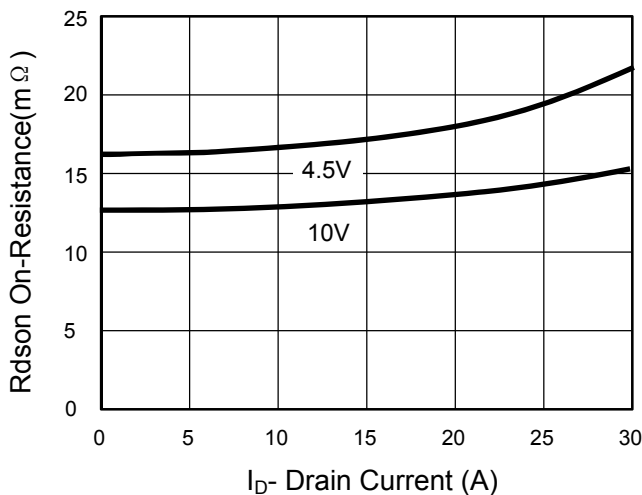


Figure 3 $R_{DS(on)}$ - Drain Current

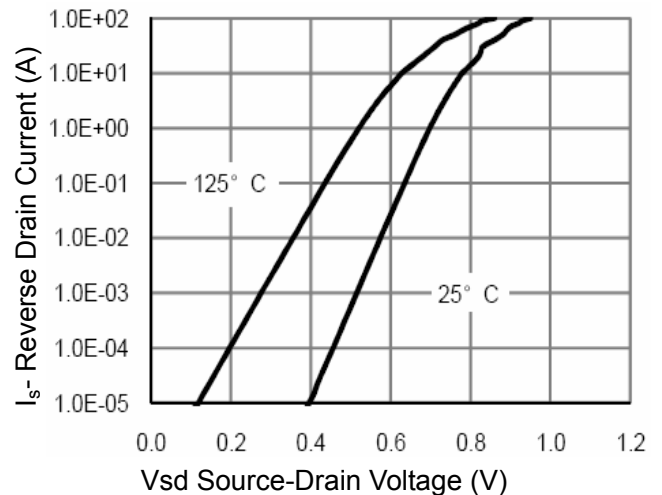


Figure 6 Source- Drain Diode Forward

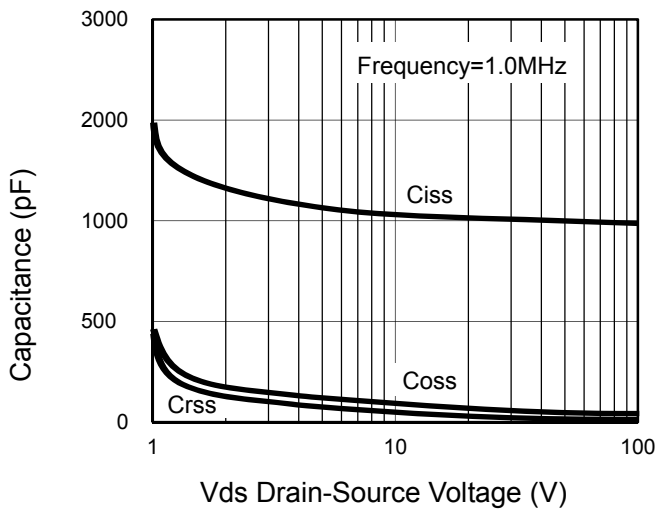


Figure 7 Capacitance vs Vds

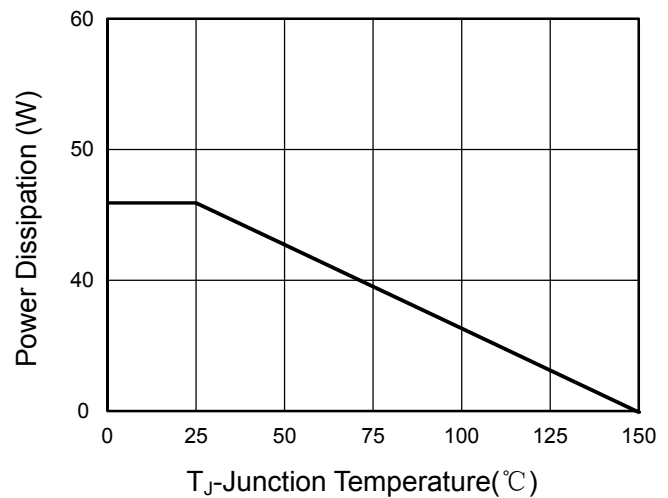


Figure 9 Power De-rating

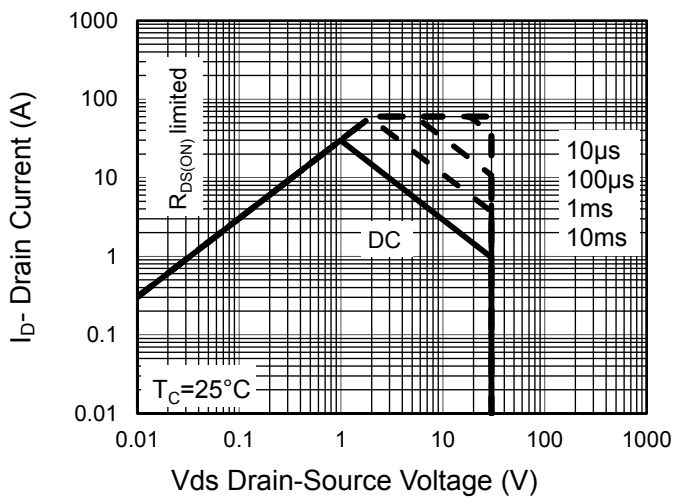


Figure 8 Safe Operation Area

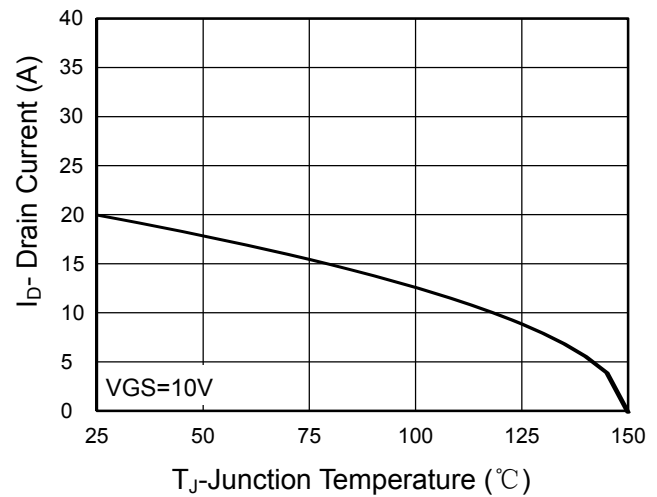


Figure 10 Current De-rating

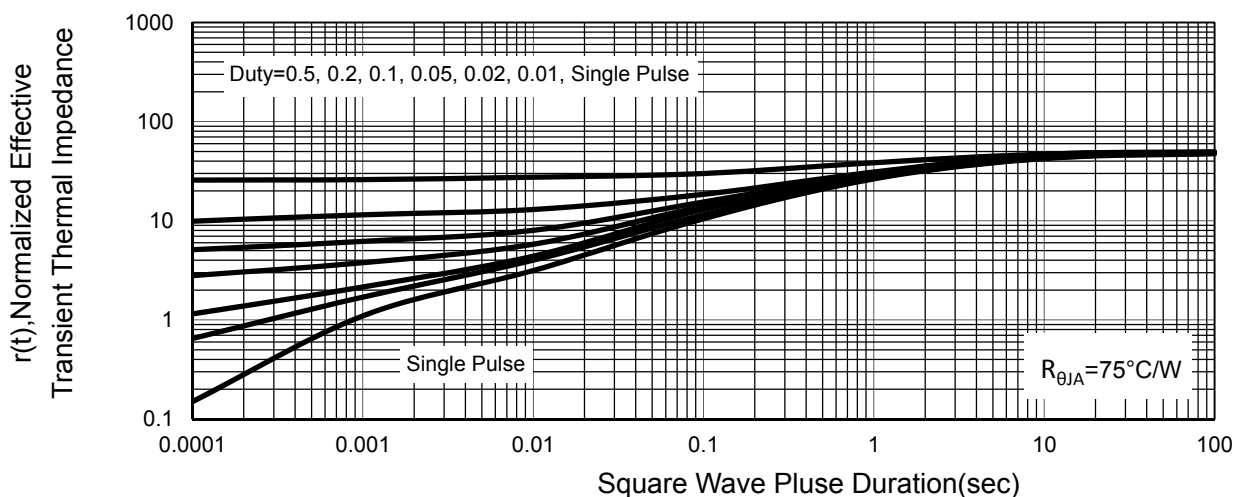
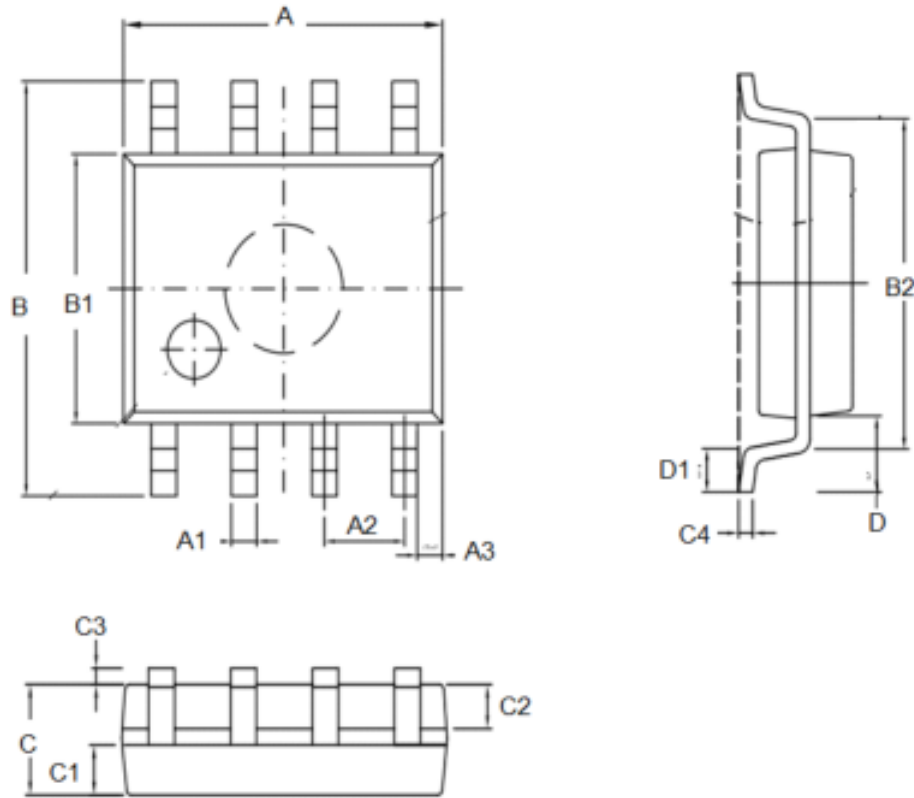


Figure 11 Normalized Maximum Transient Thermal Impedance

SOP-8L Package Outline Dimensions



Unit: mm

SYMBOL	min	TYP	max	SYMBOL	min		max
A	4.80		5.25	C	1.30		1.75
A1	0.37		0.49	C1	0.55		0.75
A2		1.27		C2	0.55		0.65
A3		0.41		C3	0.05		0.20
B	5.80		6.20	C4	0.10	0.20	0.23
B1	3.80		4.10	D		1.05	
B2		5.00		D1	0.40		0.62

Note:

1. Controlling dimension: in millimeters.

2. General tolerance: ± 0.05 mm.

3. The pad layout is for reference purposes only.