

P-Channel Enhancement Mode Power MOSFET

Description

The TF9435 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V.

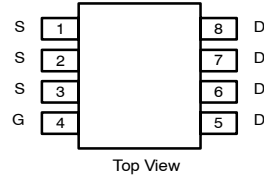
General Features

- $V_{DS} = -30V$
 $R_{DS(ON)} < 44m\Omega @ V_{GS} = -4.5V \quad I_D = -4.2A$
 $R_{DS(ON)} < 30m\Omega @ V_{GS} = -10V \quad I_D = -5.3A$
- High power and current handing capability
- Lead free product is acquired
- Surface mount package

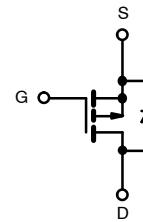
Application

- Battery Switch
- Load switch
- Power management

SOP-8



Equivalent Circuit



MARKING



Y :year code W :week code

Absolute Maximum Ratings ($T_A = 25^\circ C$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current ($T_J = 150^\circ C$)	$T_A = 25^\circ C$	I_D	-5.3	A
Drain Current-Pulsed (Note 1)		I_{DM}	-20	A
Maximum Power Dissipation		P_D	2.0	W
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 To 150	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	50	$^\circ C/W$
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SOP-8 Plastic-Encapsulate MOSFETS

TF9435

Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

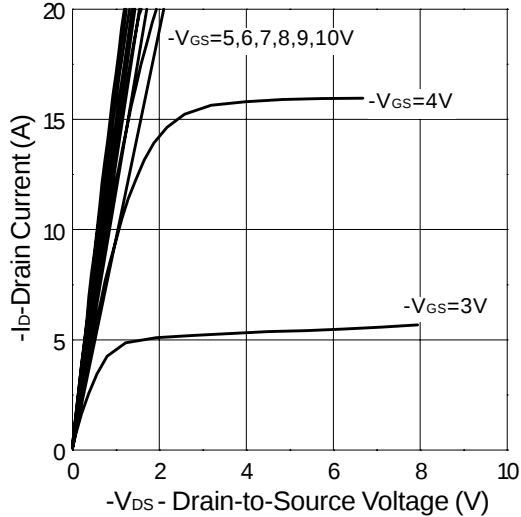
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-30	-33	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-24V, V_{GS}=0V$	-	-	-1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1	-1.5	-3.0	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=-10V, I_D=-5.3A$	-	30	40	m Ω
		$V_{GS}=-4.5V, I_D=-4.2A$	-	44	55	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=-15V, I_D=-5.3A$	10	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{iss}	$V_{DS}=-15V, V_{GS}=0V,$ $F=1.0MHz$	-	845	-	PF
Output Capacitance	C_{oss}		-	120	-	PF
Reverse Transfer Capacitance	C_{rss}		-	80	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=-25V, I_D=-2A,$ $V_{GS}=-10V, R_{GEN}=6\Omega$ $R_L=12.5\Omega$	-	17	-	nS
Turn-on Rise Time	t_r		-	18	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	60	-	nS
Turn-Off Fall Time	t_f			27	-	nS
Total Gate Charge	Q_g	$V_{DS}=-15V, I_D=-4.6A$ $V_{GS}=-10V$	-	22	-	nC
Gate-Source Charge	Q_{gs}		-	4.5	-	nC
Gate-Drain Charge	Q_{gd}		-	2	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	$V_{GS}=0V, I_S=-2.0A$	-	-	-1.2	V

Notes:

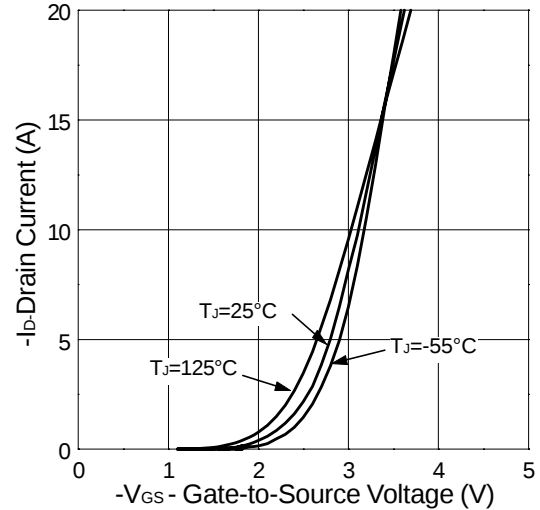
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production

Typical Characteristics

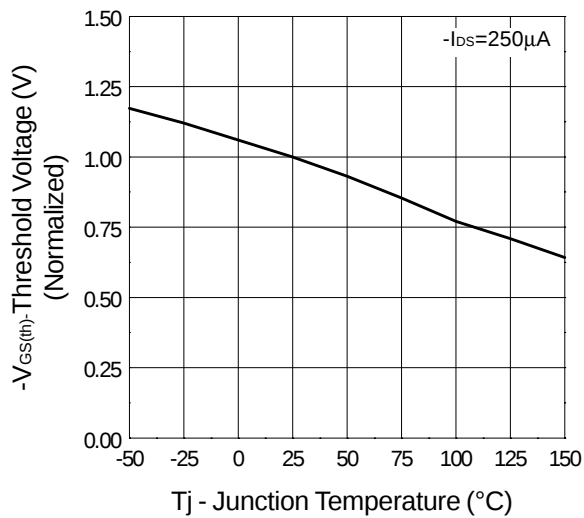
Output Characteristics



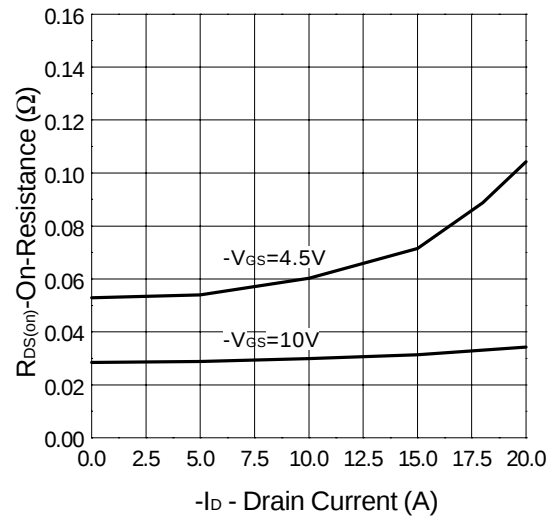
Transfer Characteristics



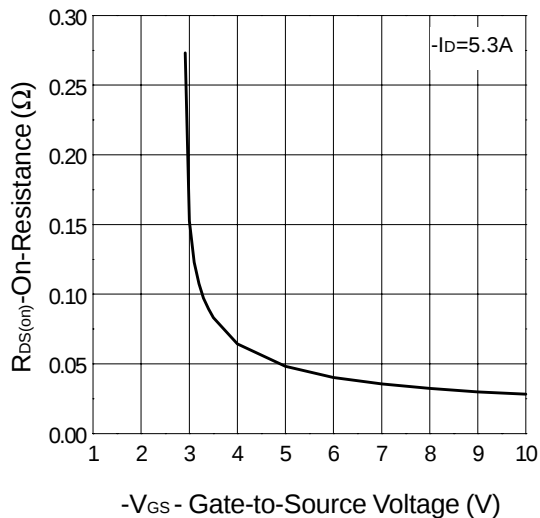
Threshold Voltage vs. Junction Temperature



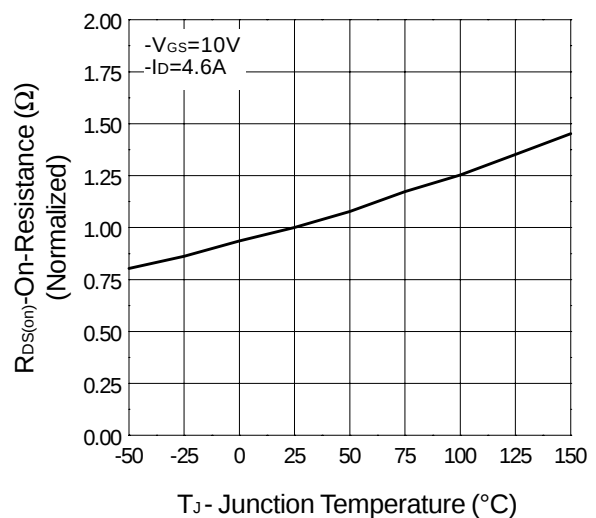
On-Resistance vs. Drain Current



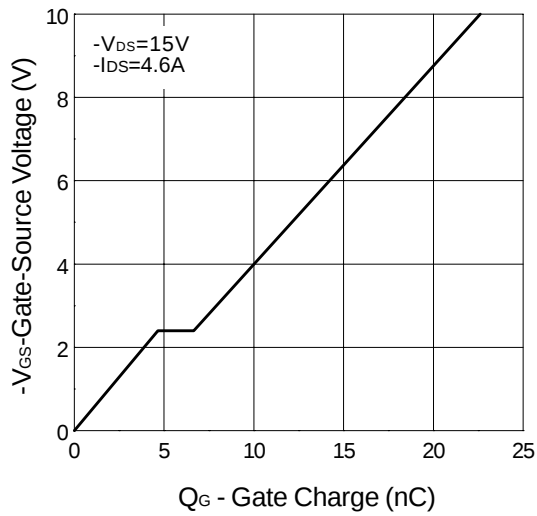
On-Resistance vs. Gate-to-Source Voltage



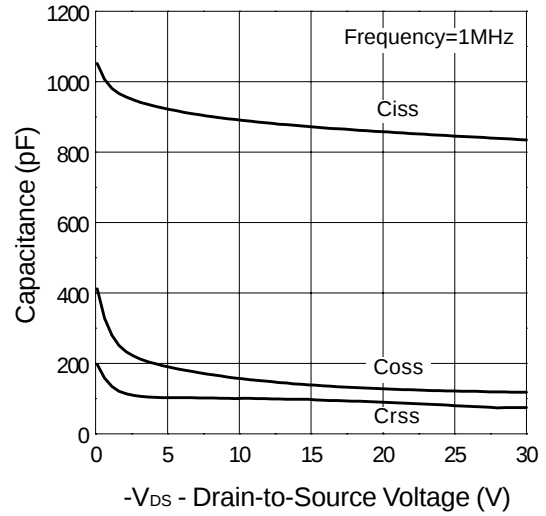
On-Resistance vs. Junction Temperature



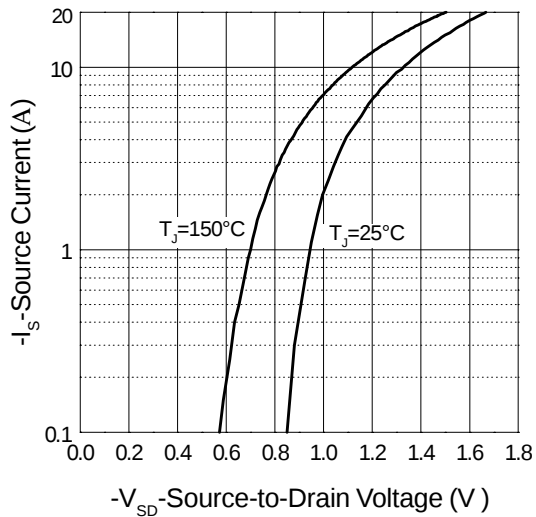
Gate Charge



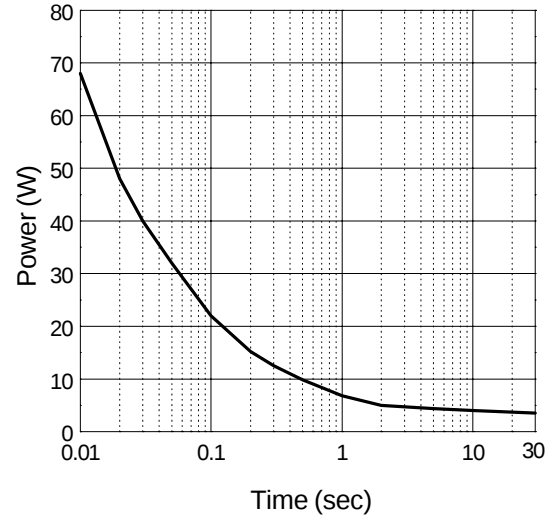
Capacitance



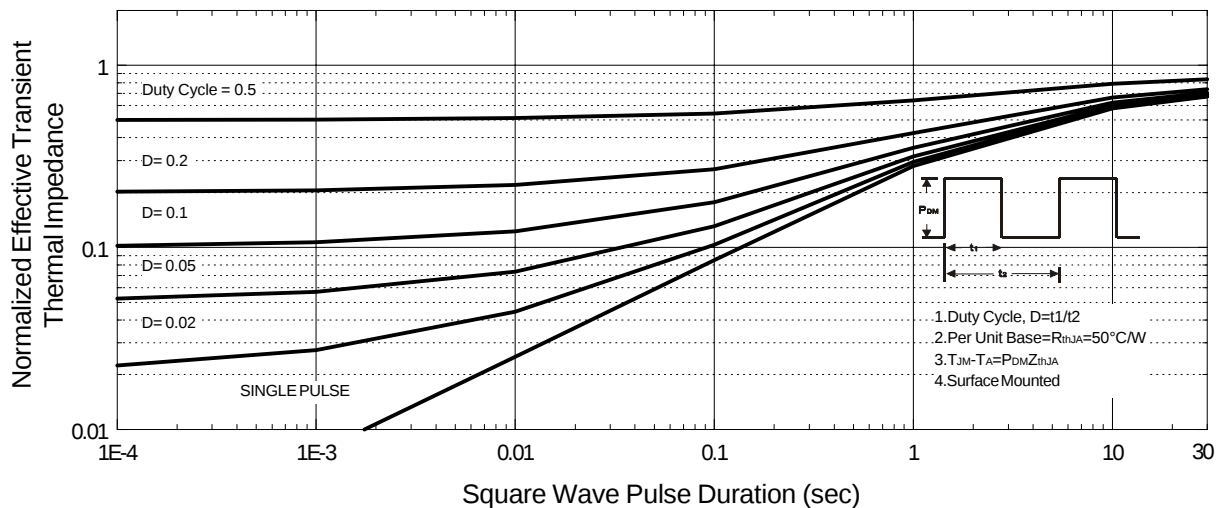
Source-Drain Diode Forward Voltage



Single Pulse Power

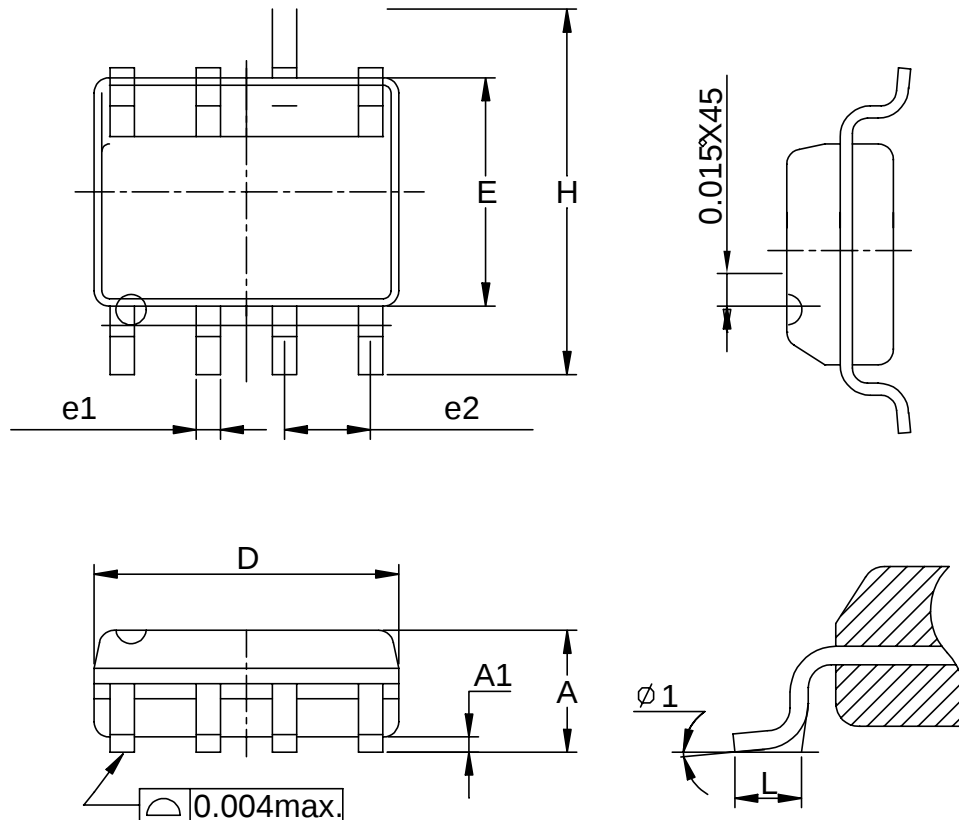


Normalized Thermal Transient Impedance, Junction to Ambient



Packaging Information

SOP-8 pin (Reference JEDEC Registration MS-012)



Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	4.80	5.00	0.189	0.197
E	3.80	4.00	0.150	0.157
H	5.80	6.20	0.228	0.244
L	0.40	1.27	0.016	0.050
e1	0.33	0.51	0.013	0.020
e2	1.27BSC		0.50BSC	
$\phi 1$	8°		8°	