



Shenzhen Tuofeng Semiconductor Technology Co., Ltd

**N-CHANNEL ENHANCEMENT MODE POWER MOSFET**

SGT MOS、低内阻、低结电容开关损耗小

**TF020N025NG****• General Description**

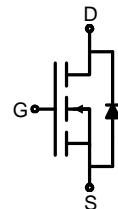
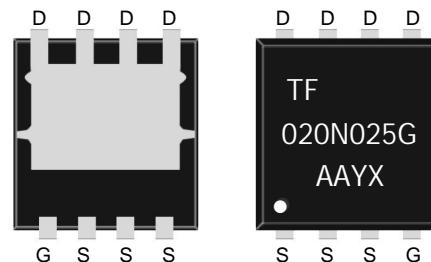
The TF020N025NG combines advanced trench MOSFET technology with a low resistance package to provide extremely low  $R_{DS(ON)}$ . This device is ideal for load switch and battery protection applications.

**• Features**

- Advance high cell density Trench technology
- Low  $R_{DS(ON)}$  to minimize conductive loss
- Low Gate Charge for fast switching
- Low Thermal resistance

**• Application**

- MB/VGA Vcore
- SMPS 2<sup>nd</sup> Synchronous Rectifier
- POL application
- BLDC Motor driver

**• Product Summary** $V_{DS} = 25V \quad I_D = 100A$  $R_{DS(on)(4.5V\ typ)} = 2.0m\Omega$  $R_{DS(on)(2.5V\ typ)} = 3.9m\Omega$ **PDFNWB5x6-8L****• Ordering Information:**

Part NO.	TF020N025NG
Marking 1	020N025G:TF020N025NG
Marking 2	TF:tuofeng; AA:device code; Y:year code; X:Week
MOQ	5000

**• Absolute Maximum Ratings ( $T_C = 25^\circ C$ )**

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	$V_{DS}$	25	V
Gate-Source Voltage	$V_{GS}$	$\pm 12$	V
Continuous Drain Current	$I_D @ T_C = 25^\circ C$	110	A
	$I_D @ T_C = 75^\circ C$	70	A
	$I_D @ T_C = 100^\circ C$	60	A
Pulsed Drain Current <sup>①</sup>	$I_{DM}$	200	A
Total Power Dissipation	$P_D @ T_C = 25^\circ C$	65	W
Total Power Dissipation	$P_D @ T_A = 25^\circ C$	1.0	W
Operating Junction Temperature	$T_J$	-55 to 150	$^\circ C$
Storage Temperature	$T_{STG}$	-55 to 150	$^\circ C$

Note: ① Pulse Test : Pulse width  $\leq 300\mu s$ , Duty cycle  $\leq 2\%$  ;



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Single Pulse Avalanche Energy	$E_{AS}$	75	mJ
Avalanche Current	$I_{AS} I_{AR}$	25	A

**•Thermal resistance**

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance, junction - case	$R_{thJC}$	-	-	2.2	° C/W
Thermal resistance, junction - ambient	$R_{thJA}$	-	-	55	° C/W
Soldering temperature, wave soldering for 8s	$T_{sold}$	-	-	265	° C

**•Electronic Characteristics( $T_a = 25^\circ\text{C}$ )**

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$	25			V
Gate Threshold Voltage	$V_{GS(\text{TH})}$	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	0.5	1.0	1.5	V
Drain-Source Leakage Current	$I_{DSS}$	$V_{DS}=25\text{V}, V_{GS} = 0\text{V}$			1.0	$\mu\text{A}$
Gate- Source Leakage Current	$I_{GSS}$	$V_{GS}=\pm 12\text{V}, V_{DS} = 0\text{V}$			$\pm 100$	nA
Static Drain-source On Resistance	$R_{DS(\text{ON})}$	$V_{GS}=4.5\text{V}, I_D=20\text{A}$		2.0	3.0	$\text{m}\Omega$
		$V_{GS}=2.5\text{V}, I_D=20\text{A}$		3.9	5.5	$\text{m}\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS} = 25\text{V}, I_D=20\text{A}$		10		S
Source-drain voltage	$V_{SD}$	$I_S=20\text{A}$			1.20	V

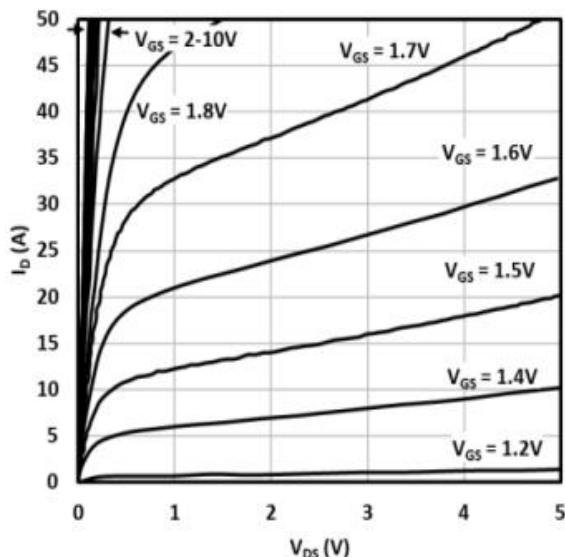
**•Electronic Characteristics( $T_a = 25^\circ\text{C}$ )**

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Input capacitance	$C_{iss}$	$V_{DS}=15\text{V}, V_{GS}=0\text{V}$ $f = 1\text{MHz}$	-	3611	-	pF
Output capacitance	$C_{oss}$		-	1856	-	
Reverse transfer capacitance	$C_{rss}$		-	73	-	

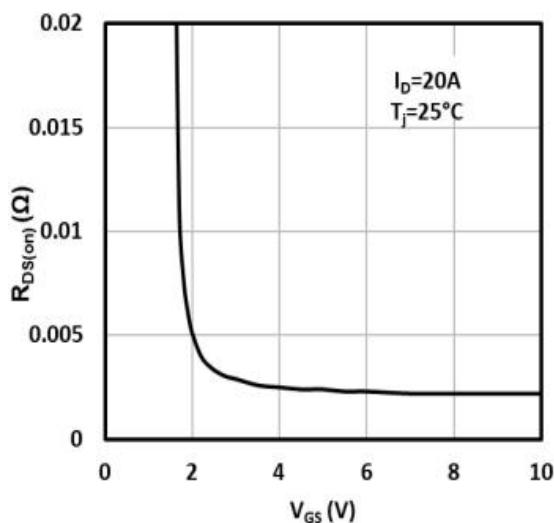
**•Gate Charge characteristics( $T_a = 25^\circ\text{C}$ )**

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Gate Resistance	$R_g$	$f = 1\text{MHz}$		1.5		$\Omega$
Total gate charge	$Q_g$	$V_{DD} = 15\text{V}$ $I_D = 20\text{A}$ $V_{GS} = 4.5\text{V}$	-	28.18	-	nC
Gate - Source charge	$Q_{gs}$		-	5.6	-	
Gate - Drain charge	$Q_{gd}$		-	6.6	-	
Turn-ON Delay time	$t_{D(on)}$	$V_{GS}=4.5\text{V}, V_{DS}=15\text{V}$ $R_G = 3.0\Omega, I=20\text{A}$		12.8		ns
Turn-ON Rise time	$t_r$			4.00		ns
Turn-Off Delay time	$t_{D(off)}$			32.0		ns
Turn-Off Fall time	$t_f$			8.00		ns

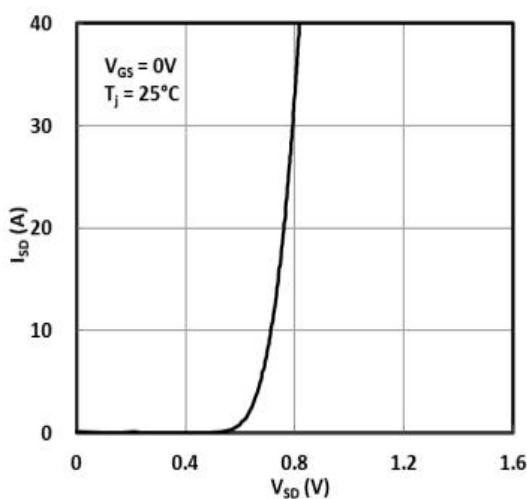
**Figure 1 Output Characteristics**



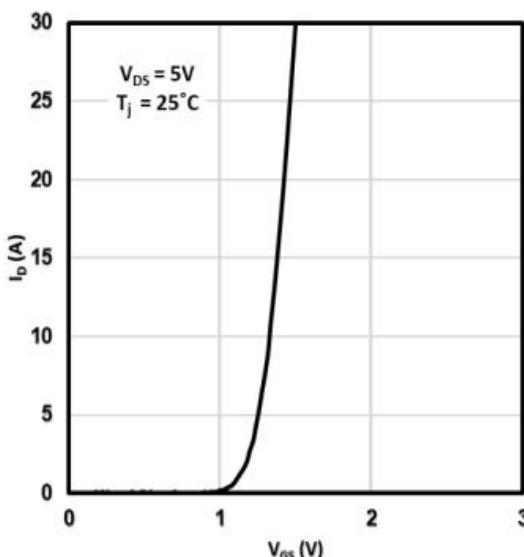
**Figure 3 On-resistance vs.gate voltage**



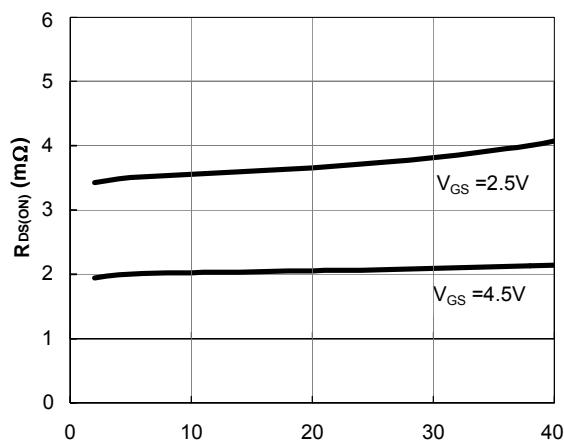
**Figure 5 Source-to-drain diode forwrd characteristics**



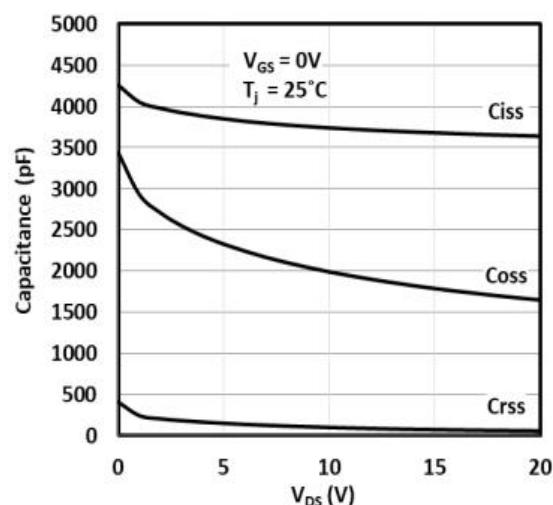
**Figure 2 Transfer Characteristics**



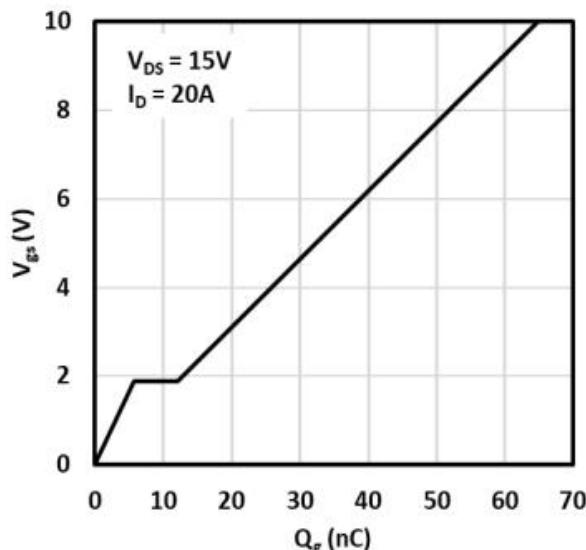
**Figure 4 On-resistance vs.drain current**



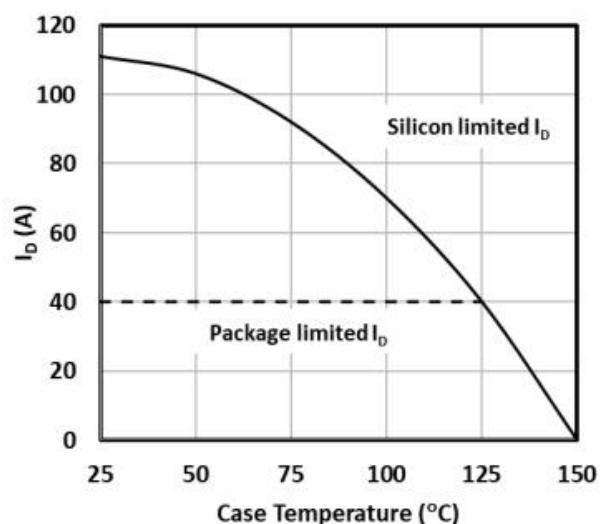
**Figure 6 Capacitance vs drain-to-source Voltage**



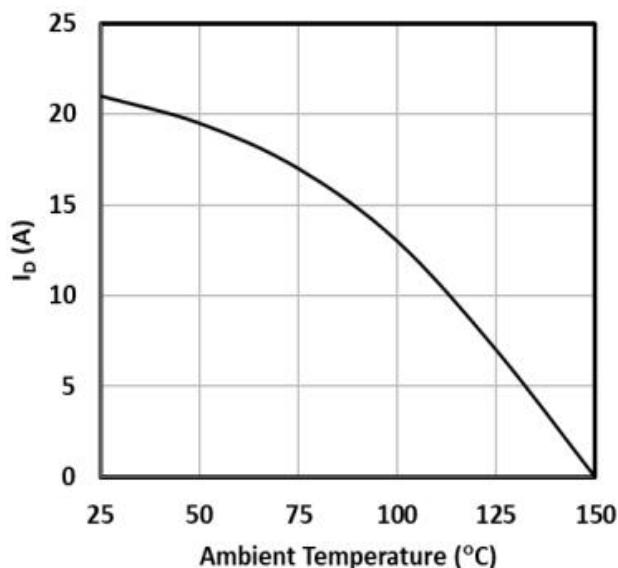
**Figure 7 Gate-to-source voltage vs.gate charge**



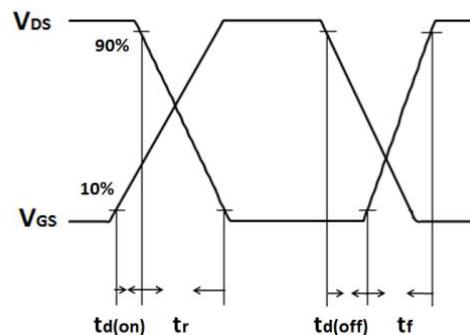
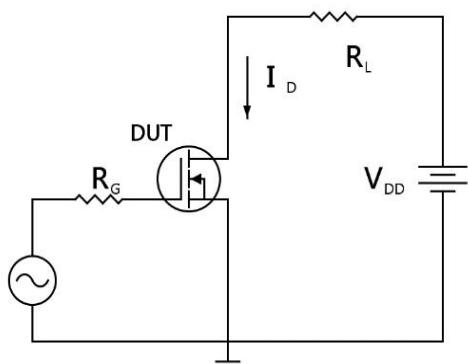
**Figure 8 Maximum drain current vs.case temperature**



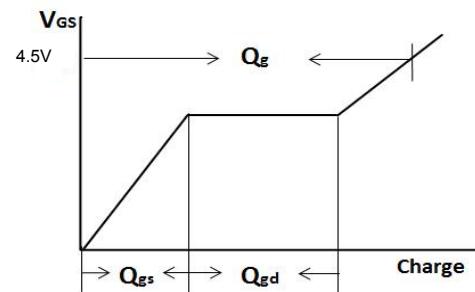
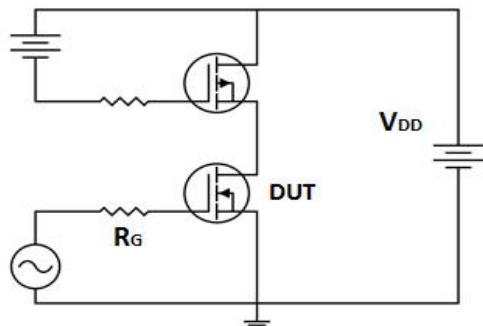
**Figure 9 Maximum drain current vs. ambient temperature**



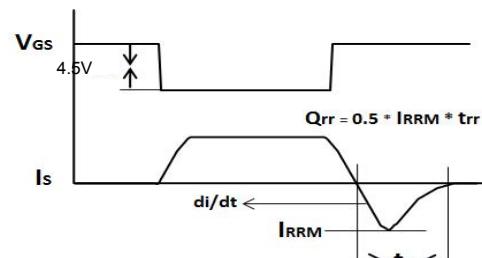
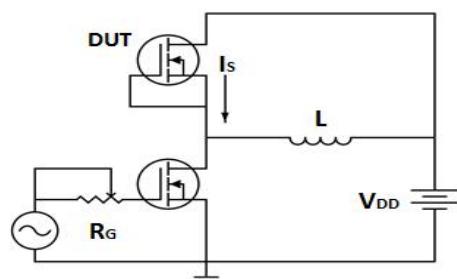
### Resistive switching time test circuit &waveforms



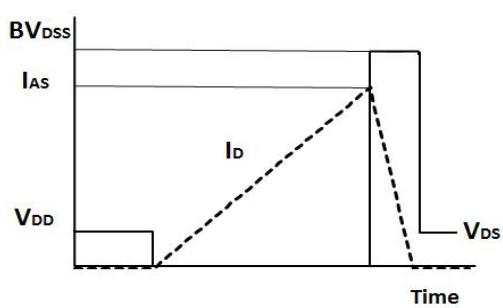
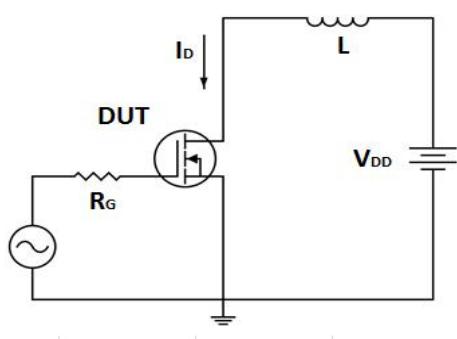
### Gate charge test circuit &waveforms



### Peak diode recovery dv/dt circuit &waveforms



### Unclamped inductive switching test circuit &waveforms





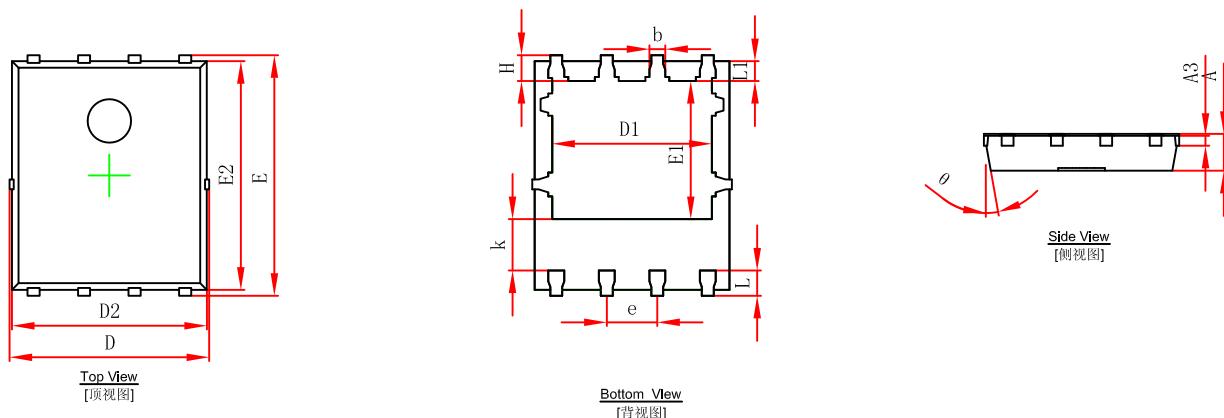
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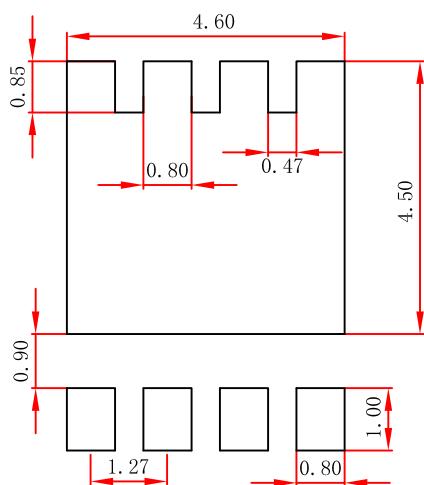
**TF020N025NG**

### PDFNWB5x6-8L Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
$\theta$	10°	12°	10°	12°

### PDFNWB5x6-8L Suggested Pad Layout



#### Note:

1. Controlling dimension: in millimeters.
2. General tolerance:  $\pm 0.05\text{mm}$ .
3. The pad layout is for reference purposes only.