

General Description

The TF050N04MG combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. This device is ideal for load switch and battery protection applications.

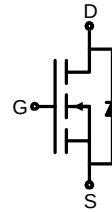
Features

- Advance high cell density Trench technology
- Low $R_{DS(ON)}$ to minimize conductive loss
- Low Gate Charge for fast switching
- Low Thermal resistance

Application

- MB/VGA Vcore
- SMPS 2nd Synchronous Rectifier
- POL application
- BLDC Motor driver

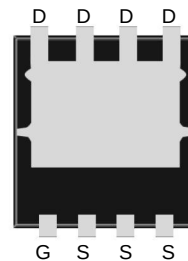
Product Summary



$$V_{DS} = 40V \quad I_D = 50A$$

$$R_{DS(ON)}(10V \text{ typ}) = 4.8m\Omega$$

$$R_{DS(ON)}(4.5V \text{ typ}) = 7.5m\Omega$$



PDFNWB3.3x3.3-8L

Ordering Information:

Part NO.	TF050N04MG
Marking 1	050N04MG:TF050N04MG
Marking 2	TF:tuofeng; AA:device code; Y:year code; X:Week
MOQ	5000

Absolute Maximum Ratings ($T_C = 25^\circ C$)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	$I_D @ T_C = 25^\circ C$	50	A
	$I_D @ T_C = 75^\circ C$	40	A
	$I_D @ T_C = 100^\circ C$	30	A
Pulsed Drain Current ①	I_{DM}	150	A
Total Power Dissipation	$P_D @ T_C = 25^\circ C$	55	W
Total Power Dissipation	$P_D @ T_A = 25^\circ C$	2.0	W
Operating Junction Temperature	T_J	-55 to 150	$^\circ C$
Storage Temperature	T_{STG}	-55 to 150	$^\circ C$

Note: ① Pulse Test : Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$;



Shenzhen Tuofeng Semiconductor Technology Co., Ltd

N-CHANNEL ENHANCEMENT MODE POWER MOSFET

SGT MOS、低内阻、低结电容开关损耗小

TF050N04MG

Single Pulse Avalanche Energy	E _{AS}		120		mJ	
Avalanche Current	I _{AS} I _{AR}		20		A	
●Thermal resistance						
Parameter		Symbol	Min.	Typ.	Max.	Unit
Thermal resistance, junction - case		R _{thJC}	-	-	3.2	° C/W
Thermal resistance, junction - ambient		R _{thJA}	-	-	57	° C/W
Soldering temperature, wave soldering for 8s		T _{sold}	-	-	265	° C
●Electronic Characteristics						
Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250uA	40			V
Gate Threshold Voltage	V _{GS(TH)}	V _{GS} =V _{DS} , I _D =250uA	1.0	1.5	2.5	V
Drain-Source Leakage Current	I _{DSS}	V _{DS} =40V, V _{GS} =0V			1.0	uA
Gate- Source Leakage Current	I _{GSS}	V _{GS} =±20V ,V _{DS} =0V			±100	nA
Static Drain-source On Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =20A		4.8	6.5	mΩ
		V _{GS} =4.5V, I _D =15A		7.5	9.0	mΩ
Forward Transconductance	g _{FS}	V _{DS} =25V, I _D =20A		10		S
Source-drain voltage	V _{SD}	IS=20A			1.20	V
●Electronic Characteristics						
Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Input capacitance	Ciss	Vds=20V,Vgs=0V f = 1MHz	-	1048	-	pF
Output capacitance	Coss		-	187	-	
Reverse transfer capacitance	Crss		-	178	-	
●Gate Charge characteristics(T _a = 25°C)						
Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Gate Risistance	R _g	f = 1MHz		1.5		Ω
Total gate charge	Qg	V _{DD} = 20V I _D = 20A V _{GS} = 10V	-	28.0	-	nC
Gate - Source charge	Qgs		-	4.00	-	
Gate - Drain charge	Qgd		-	6.00	-	
Turn-ON Delay time	t _{D(on)}	V _{GS} =10V ,V _{DS} =20V R _G =3.0Ω, I=20A		4.80		ns
Turn-ON Rise time	t _r			57.0		ns
Turn-Off Delay time	t _{D(off)}			17.8		ns
Turn-Off Fall time	t _f			51.0		ns

Fig.1 Power Dissipation

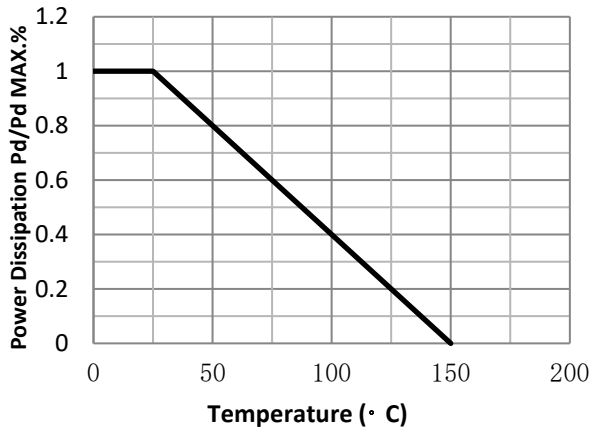


Fig.2 Typical output Characteristics

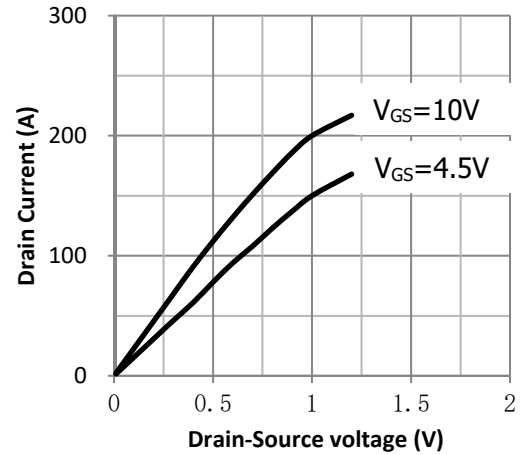


Fig.3 Threshold Voltage V.S Junction Temperature

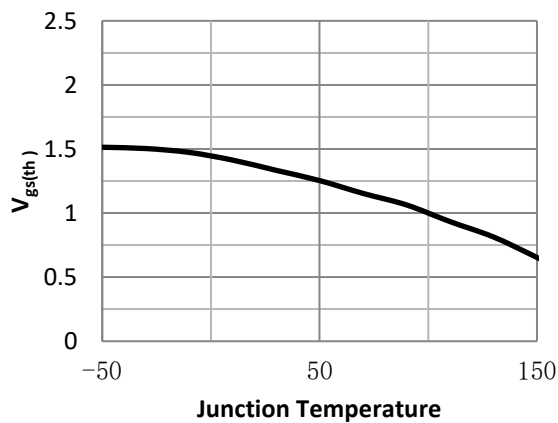


Fig.4 Resistance V.S Drain Current

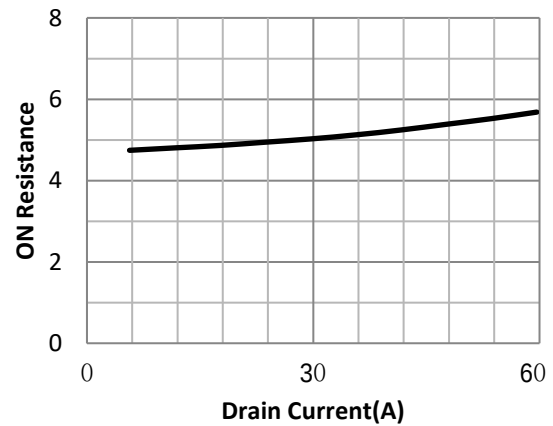


Fig.5 On-Resistance VS Gate Source Voltage

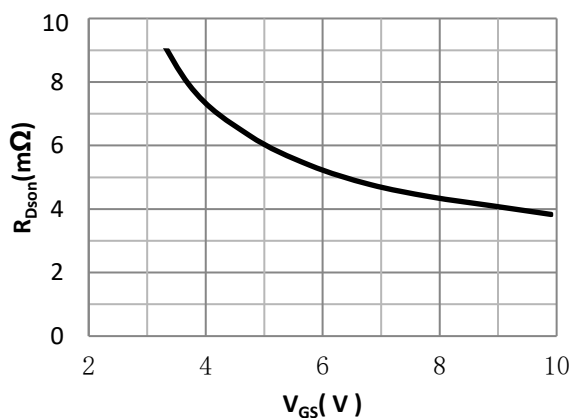


Fig.6 On-Resistance V.S Junction Temperature

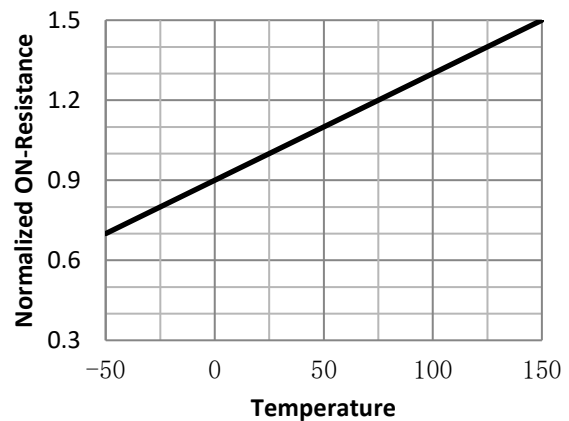


Fig.7 Switching Time Measurement Circuit

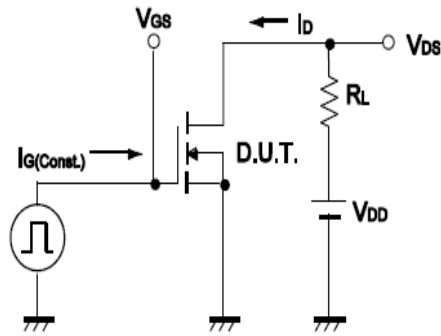


Fig.8 Gate Charge Waveform

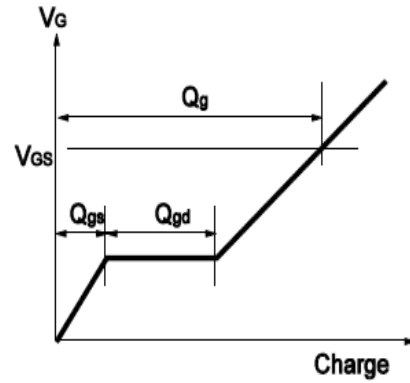


Fig.9 Switching Time Measurement Circuit

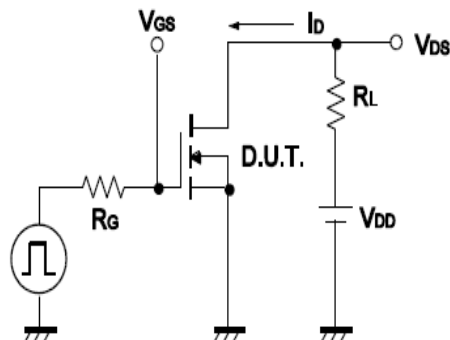


Fig.10 Gate Charge Waveform

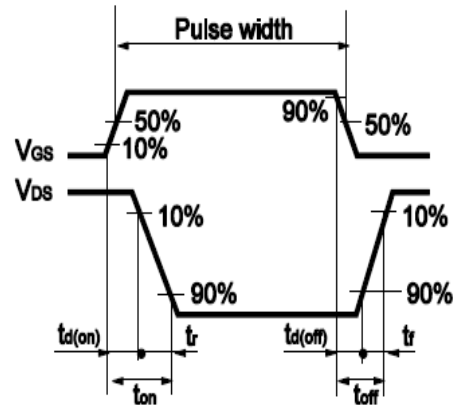


Fig.11 Avalanche Measurement Circuit

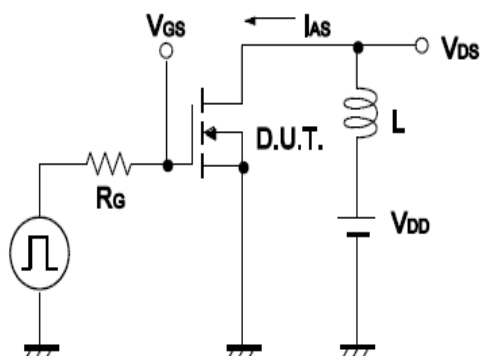
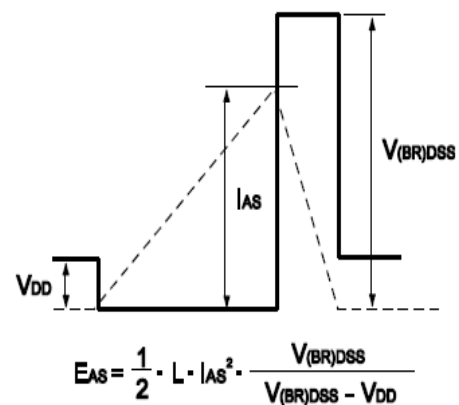
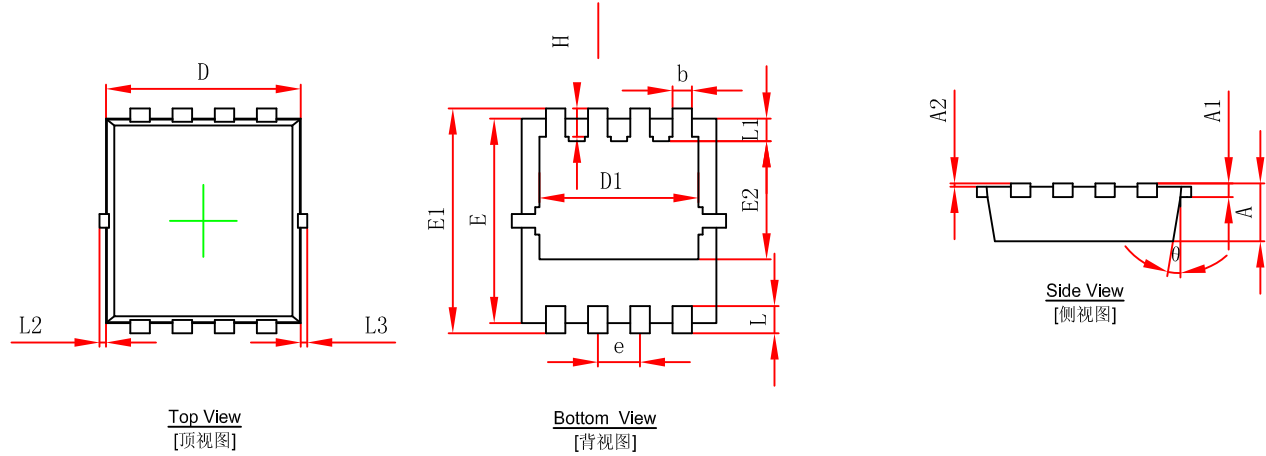


Fig.12 Avalanche Waveform

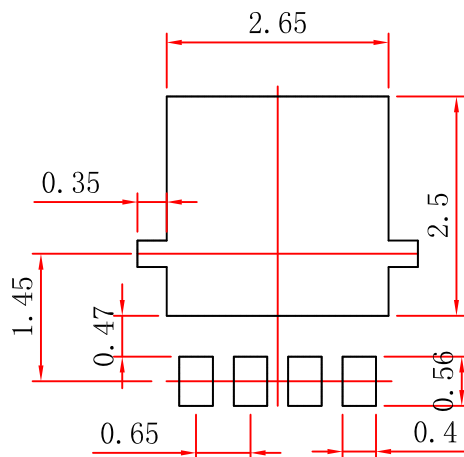


PDFNWB3.3x3.3-8L Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.650	0.850	0.026	0.033
A1	0.152 REF.		0.006 REF.	
A2	0~0.05		0~0.002	
D	2.900	3.100	0.114	0.122
D1	2.300	2.600	0.091	0.102
E	2.900	3.100	0.114	0.122
E1	3.150	3.450	0.124	0.136
E2	1.535	1.935	0.060	0.076
b	0.200	0.400	0.008	0.016
e	0.550	0.750	0.022	0.030
L	0.300	0.500	0.012	0.020
L1	0.180	0.480	0.007	0.019
L2	0~0.100		0~0.004	
L3	0~0.100		0~0.004	
H	0.315	0.515	0.012	0.020
θ	9°	13°	9°	13°

PDFNWB3.3x3.3-8L Suggested Pad Layout



Note:

1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.05\text{mm}$.
3. The pad layout is for reference purposes only.