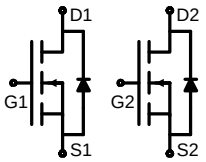
TFD040N03N

● General Description

The TFD040N03N combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$ .This device is ideal for load switch and battery protection applications.

● Product Summary



V_{DS} =30V I_D=60A

$R_{DSON(10V\ typ)}$ =5.5mΩ

$R_{DSON(4.5V\ typ)}$ =7.3mΩ

● Features

Advance high cell density Trench technology

Low $R_{DS(ON)}$ to minimize conductive loss

Low Gate Charge for fast switching

Low Thermal resistance

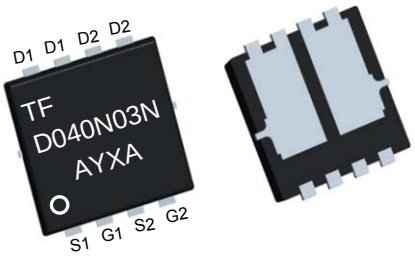
●Application

MB/VGA Vcore

SMPS 2nd Synchronous Rectifier

POL application

BLDC Motor driver



PDFNWB5x6-8L

●Ordering Information:

Part NO.	TFD040N03N
Marking 1	D040N03N
Marking 2	TF:tuofeng; AA:device code; Y:year code; X:Week
MOQ	5000

●Absolute Maximum Ratings (T_C =25℃)

Parameter	**Symbol**	Rating	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current	$I_{D@}T_C$=25℃	60	A
	$I_{D@}T_C$=75℃	42	A
	$I_{D\ @}T_C$=100℃	36	A
Pulsed Drain Current ①	I_{DM}	180	A
Total Power Dissipation	$P_D@T_C$=25℃	50	W
Total Power Dissipation	$P_D@T_A$=25℃	2.0	W
Operating Junction Temperature	T_J	-55 to 150	℃
Storage Temperature	T_{STG}	-55 to 150	℃

Note: ① Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2% ;

Single Pulse Avalanche Energy	E_{AS}	90	mJ
Avalanche Current	I_{AS} I_{AR}	20	A

●Thermal resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance, junction - case	R_{thJC}	-	-	4.3	° C/W
Thermal resistance, junction - ambient	R_{thJA}	-	-	58	° C/W
Soldering temperature, wave soldering for 8s	T_{sold}	-	-	265	° C

●Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} =0V,I_D =250uA	30			V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} =V_{DS}, I_D =250uA	1.0	1.5	2.5	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=30V, V_{GS} =0V			1.0	uA
Gate- Source Leakage Current	I_{GSS}	V_{GS}=±20V ,V_{DS} =0V			±100	nA
Static Drain-source On Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=20A		5.5	7.0	mΩ
		V_{GS}=4.5V, I_D=15A		7.3	9.0	mΩ
Forward Transconductance	g_{FS}	V_{DS} =25V, I_D=20A		15		S
Source-drain voltage	V_{SD}	Is=20A			1.20	V

●Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Input capacitance	Ciss	Vds=15V,Vgs=0V f = 1MHz	-	2700	-	pF
Output capacitance	Coss		-	321	-	
Reverse transfer capacitance	Crss		-	245	-	

●Gate Charge characteristics(T_a = 25℃)

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Gate Risistance	R_g	f = 1MHz		1.5		Ω
Total gate charge	Qg	V_{DD} = 15V	-	42	-	nC
Gate - Source charge	Qgs	I_D = 20A	-	4.0	-	
Gate - Drain charge	Qgd	V_{GS} = 10V	-	14	-	
Turn-ON Delay time	$t_{D(on)}$	V_{GS}=10V ,V_{DS}=10V R_G =3.0Ω, I=20A		13		ns
Turn-ON Rise time	t_r			36		ns
Turn-Off Delay time	$t_{D(off)}$			43		ns
Turn-Off Fall time	t_f			16		ns

Fig.1 Power Dissipation

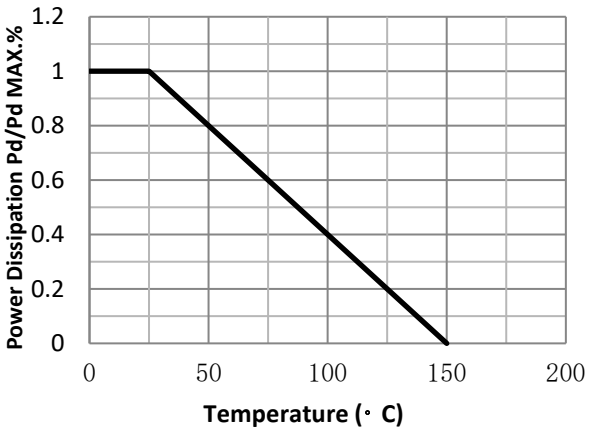


Fig.2 Typical output Characteristics

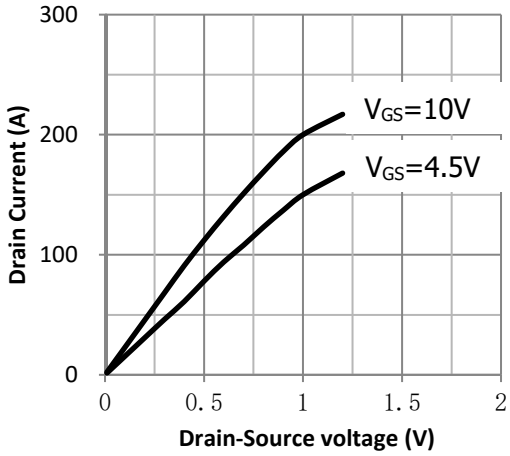


Fig.3 Threshold Voltage V.S Junction Temperature

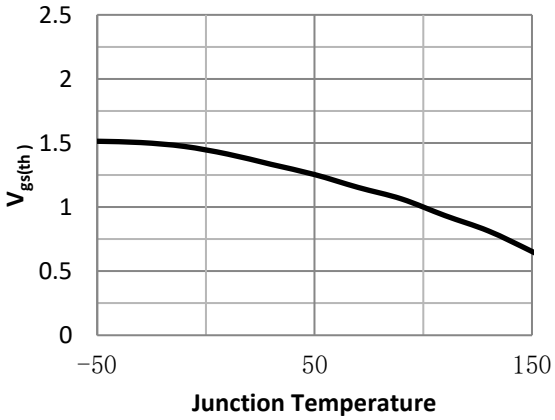


Fig.4 Resistance V.S Drain Current

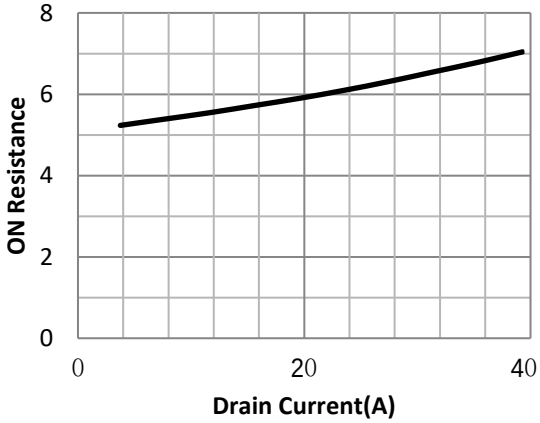


Fig.5 On-Resistance VS Gate Source Voltage

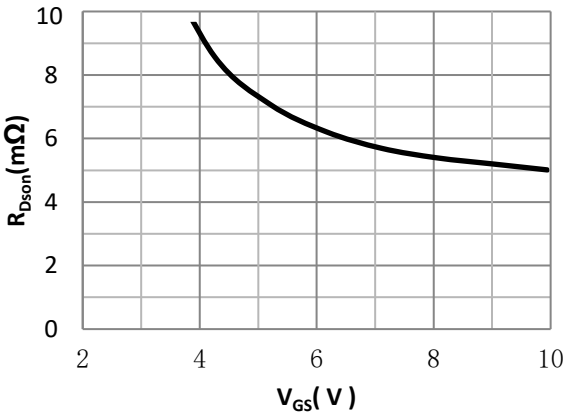


Fig.6 On-Resistance V.S Junction Temperature

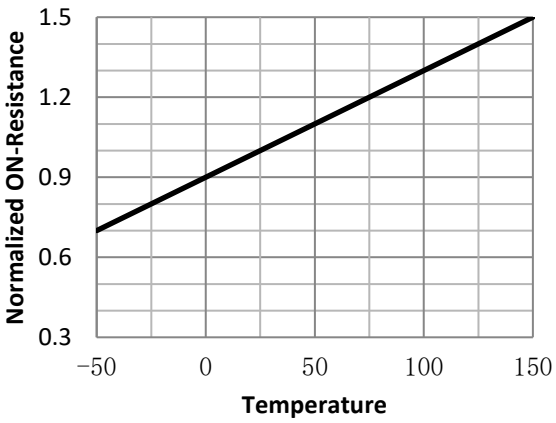


Fig.7 Switching Time Measurement Circuit

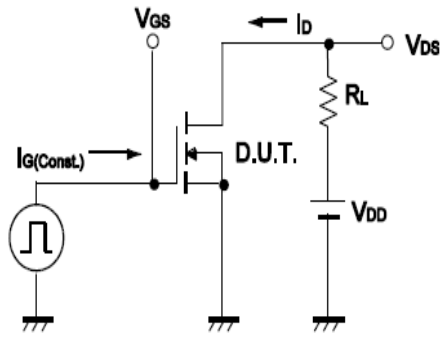


Fig.8 Gate Charge Waveform

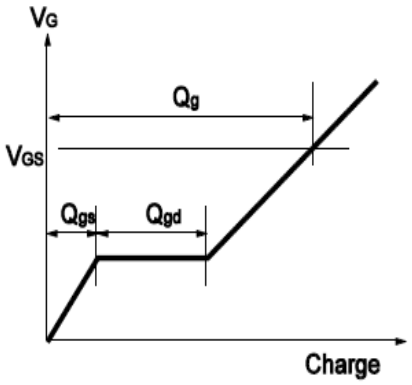


Fig.9 Switching Time Measurement Circuit

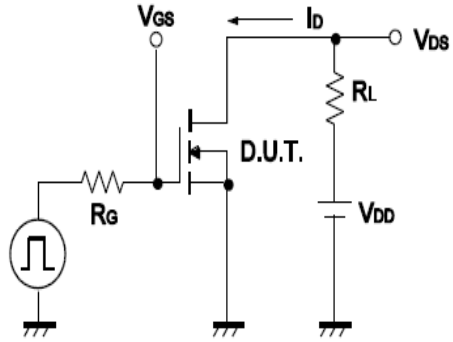


Fig.10 Gate Charge Waveform

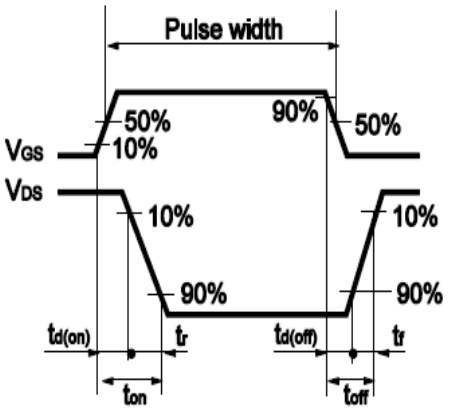


Fig.11 Avalanche Measurement Circuit

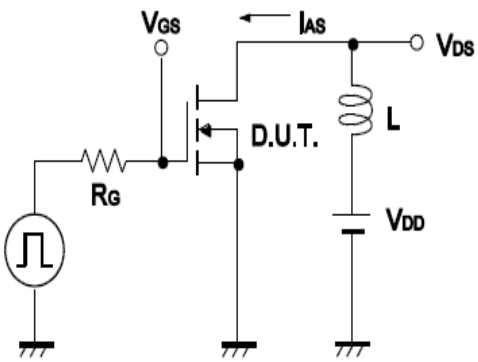
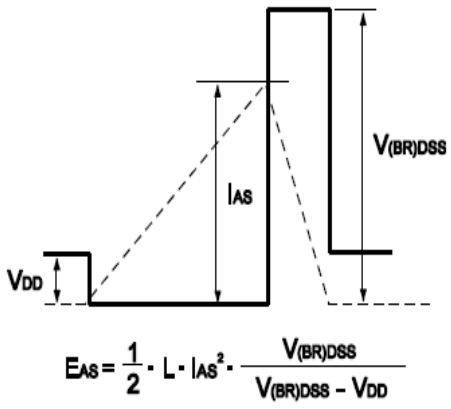
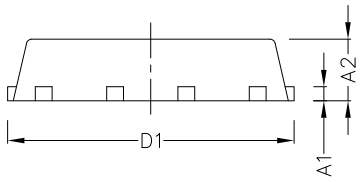


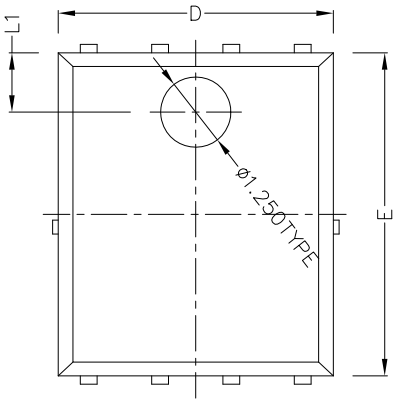
Fig.12 Avalanche Waveform



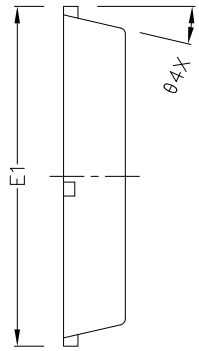
PDFNWB5x6-8L Package Outline Dimensions



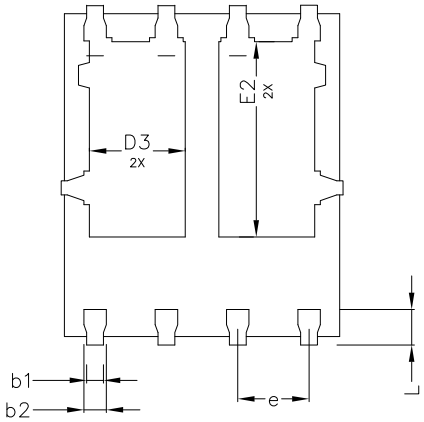
SIDE VIEW



TOP VIEW



SIDE VIEW



BOTTOM VIEW
OPTION

COMMON DIMENSIONS (UNITS OF MEASURE IS mm)			
	MIN	NORMAL	MAX
A1		0.254 BSC	
A2	1.000	1.100	1.200
b1	0.250	0.300	0.350
b2	0.350	0.400	0.450
D	4.800	4.900	5.000
D1	5.000	5.100	5.200
D2	3.910	4.010	4.110
D3	1.605	1.705	1.805
E	5.650	5.750	5.850
E1	5.950	6.050	6.150
E2	3.375	3.475	3.575
e		1.270 TYPE	
L	0.530	0.630	0.730
L1		1.00REF	
θ		13° TYPE	

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.05mm.
3.The pad layout is for reference purposes only.