## ● General Description

The TF060N04NG combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$ .This device is ideal for load switch and battery protection applications.

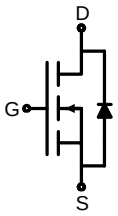
## ● Features

Advance high cell density Trench technology
Low $R_{DS(ON)}$ to minimize conductive loss
Low Gate Charge for fast switching
Low Thermal resistance

## ●Application

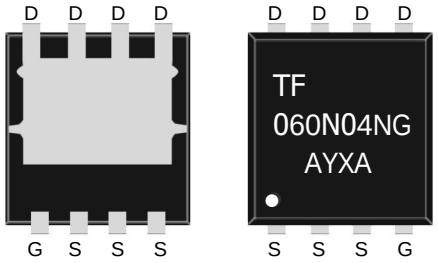
MB/VGA Vcore
SMPS 2nd Synchronous Rectifier
POL application
BLDC Motor driver

## ● Product Summary




$V_{DS}$ =40V $I_D$=50A
$R_{DSON(10V\ typ)}$ =6.0mΩ
$R_{DSON(4.5V\ typ)}$ =8.2mΩ

RoHS compliant




**PDFNWB5x6-8L**

## ●Ordering Information:

| | |
|---|---|
| Part NO. | TF060N04NG |
| Marking 1 | 060N04NG |
| Marking 2 | TF:tuofeng; AA:device code; Y:year code; X:Week |
| MOQ | 5000 |

## ●Absolute Maximum Ratings ($T_C$ =25℃)

| **Parameter** | **Symbol** | Rating | Unit |
|---|---|---|---|
| Drain-Source Voltage | $V_{DS}$ | 40 | V |
| Gate-Source Voltage | $V_{GS}$ | ±20 | V |
| Continuous Drain Current | $I_{D@}T_C$=25℃ | 50 | A |
| | $I_{D@}T_C$=75℃ | 42 | A |
| | $I_{D\ @}T_C$=100℃ | 30 | A |
| Pulsed Drain Current ① | $I_{DM}$ | 180 | A |
| Total Power Dissipation | $P_D$@$T_C$=25℃ | 45 | W |
| Total Power Dissipation | $P_D$@$T_A$=25℃ | 2.0 | W |
| Operating Junction Temperature | $T_J$ | -55 to 150 | ℃ |
| Storage Temperature | $T_{STG}$ | -55 to 150 | ℃ |

Note: ① Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2% ;

| | | | |
|---|---|---|---|
| Single Pulse Avalanche Energy | $E_{AS}$ | 39 | mJ |
| Avalanche Current | $I_{AS}$ $I_{AR}$ | 15 | A |

**●Thermal resistance**

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Thermal resistance, junction - case | $R_{thJC}$ | - | - | 4.5 | °C/W |
| Thermal resistance, junction - ambient | $R_{thJA}$ | - | - | 60 | °C/W |
| Soldering temperature, wave soldering for 8s | $T_{sold}$ | - | - | 265 | °C |

**●Electronic Characteristics**

| Parameter | Symbol | Condition | Min. | Typ | Max. | Unit |
|---|---|---|---|---|---|---|
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | $V_{GS}$ =0V,$I_D$ =250uA | 40 | | | V |
| Gate Threshold Voltage | $V_{GS(TH)}$ | $V_{GS}$ =$V_{DS}$, $I_D$ =250uA | 1.0 | 1.7 | 2.5 | V |
| Drain-Source Leakage Current | $I_{DSS}$ | $V_{DS}$=40V, $V_{GS}$ =0V | | | 1.0 | uA |
| Gate- Source Leakage Current | $I_{GSS}$ | $V_{GS}$=±20V ,$V_{DS}$ =0V | | | ±100 | nA |
| Static Drain-source On Resistance | $R_{DS(ON)}$ | $V_{GS}$=10V, $I_D$=20A | | 6.0 | 8.0 | mΩ |
| | | $V_{GS}$=4.5V, $I_D$=15A | | 8.2 | 12 | mΩ |
| Forward Transconductance | $g_{FS}$ | $V_{DS}$ =25V, $I_D$=10A | | 15 | | S |
| Source-drain voltage | $V_{SD}$ | Is=20A | | | 1.20 | V |

**●Electronic Characteristics**

| Parameter | Symbol | Condition | Min. | Typ | Max. | Unit |
|---|---|---|---|---|---|---|
| Input capacitance | Ciss | Vds=20V,Vgs=0V f = 1MHz | - | 795 | - | pF |
| Output capacitance | Coss | | - | 168 | - | |
| Reverse transfer capacitance | Crss | | - | 12.9 | - | |

**●Gate Charge characteristics**($T_a$ = 25℃)

| Parameter | Symbol | Condition | Min. | Typ | Max. | Unit |
|---|---|---|---|---|---|---|
| Gate Risistance | $R_g$ | f = 1MHz | | 1.3 | | Ω |
| Total gate charge | Qg | $V_{DD}$ = 20V | - | 14.4 | - | nC |
| Gate - Source charge | Qgs | $I_D$ = 20A | - | 2.4 | - | |
| Gate - Drain charge | Qgd | $V_{GS}$ = 10V | - | 2.3 | - | |
| Turn-ON Delay time | $t_{D(on)}$ | $V_{GS}$=10V ,$V_{DS}$=20V $R_G$ =3.0Ω, I=20A | | 5.70 | | ns |
| Turn-ON Rise time | $t_r$ | | | 4.10 | | ns |
| Turn-Off Delay time | $t_{D(off)}$ | | | 14.7 | | ns |
| Turn-Off Fall time | $t_f$ | | | 4.00 | | ns |

## Typical Characteristics

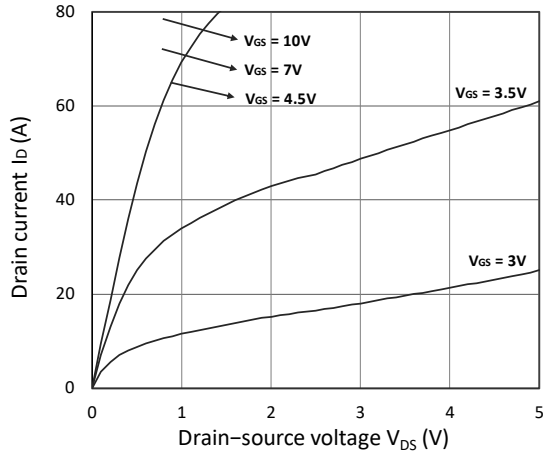



Figure 1. Output Characteristics

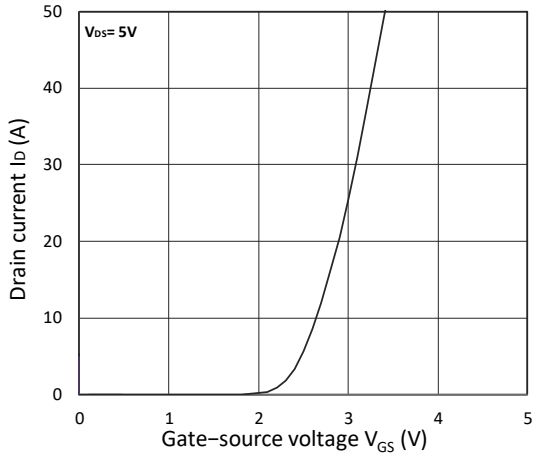



Figure 2. Transfer Characteristics

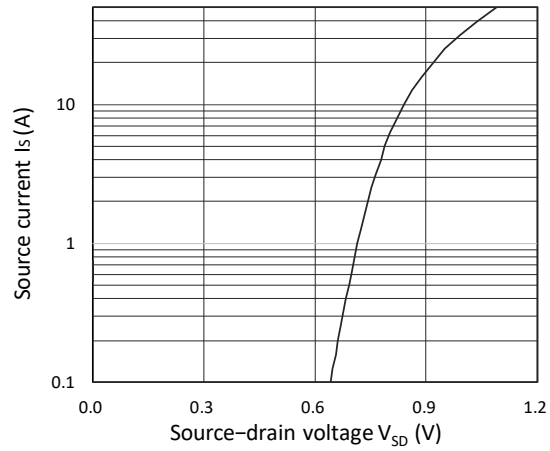



Figure 3. Forward Characteristics of Reverse

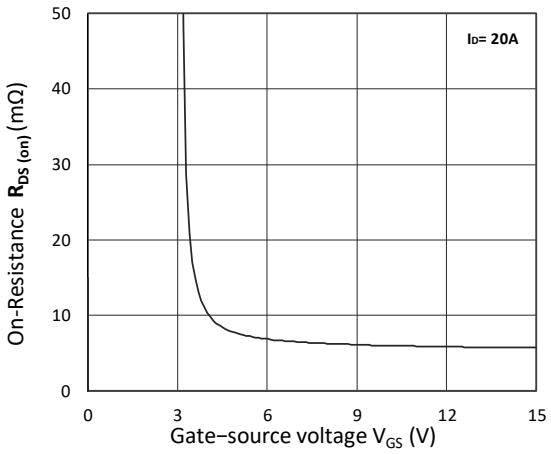



Figure 4. $R_{DS(ON)}$ vs. $V_{GS}$

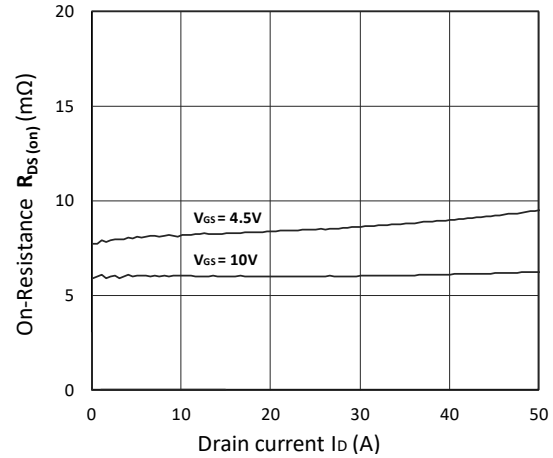



Figure 5. $R_{DS(ON)}$ vs. $I_D$

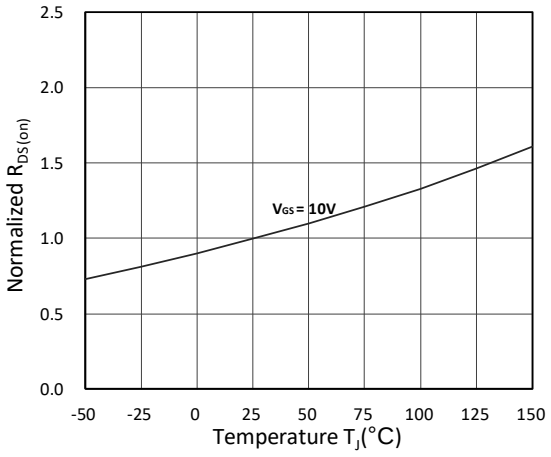



Figure 6. Normalized $R_{DS(on)}$ vs. Temperature

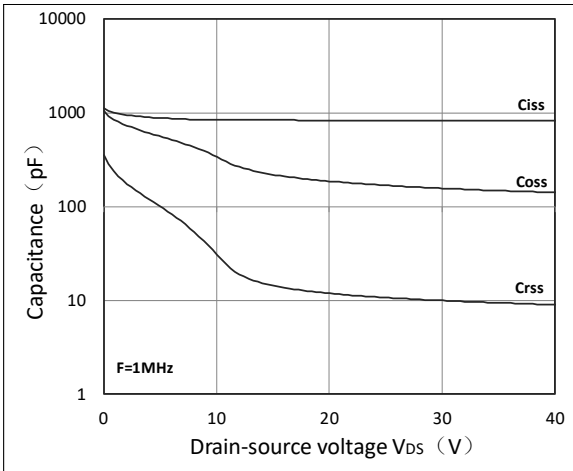



Figure 7. Capacitance Characteristics

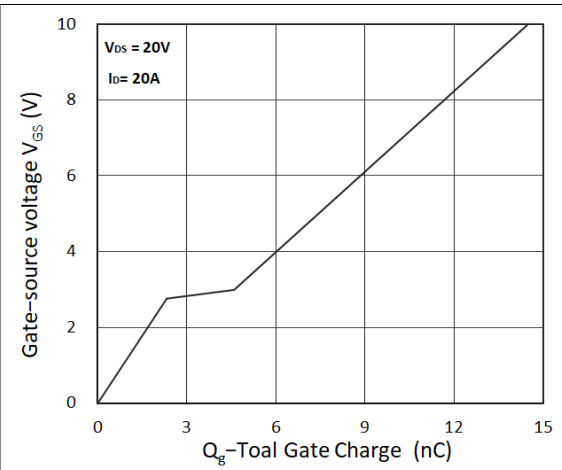



Figure 8. Gate Charge Characteristics

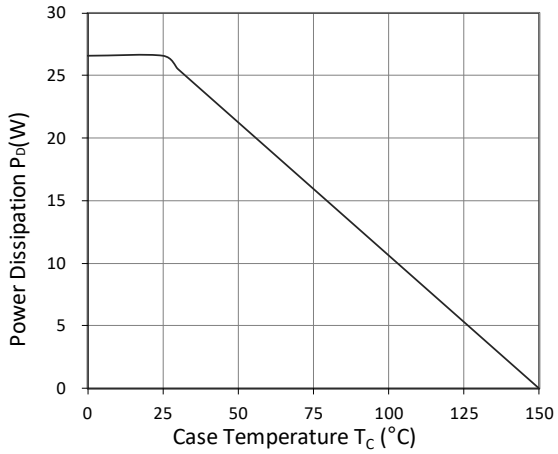



Figure 9. Power Dissipation

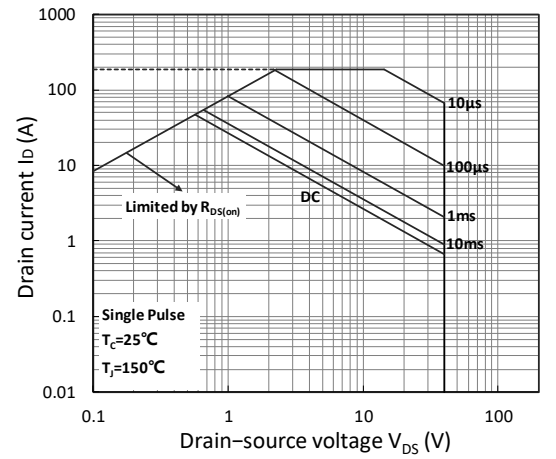



Figure10. Safe Operating Area

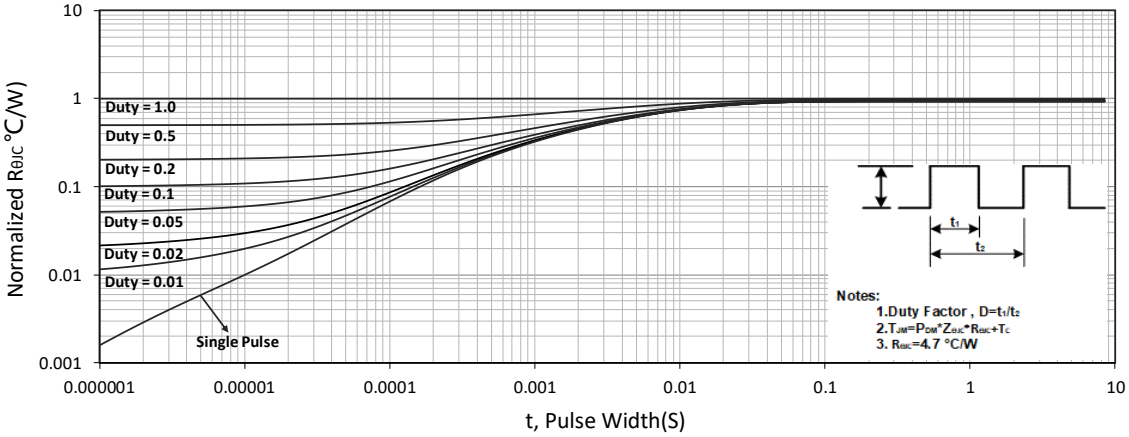



Figure 11. Normalized Maximum Transient Thermal Impedance

## Test Circuit

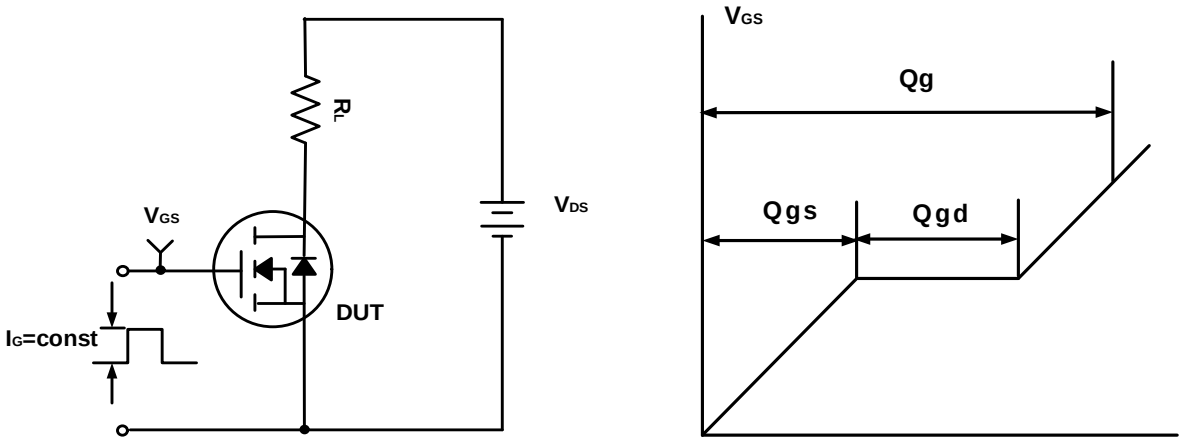



**Figure A. Gate Charge Test Circuit & Waveforms**

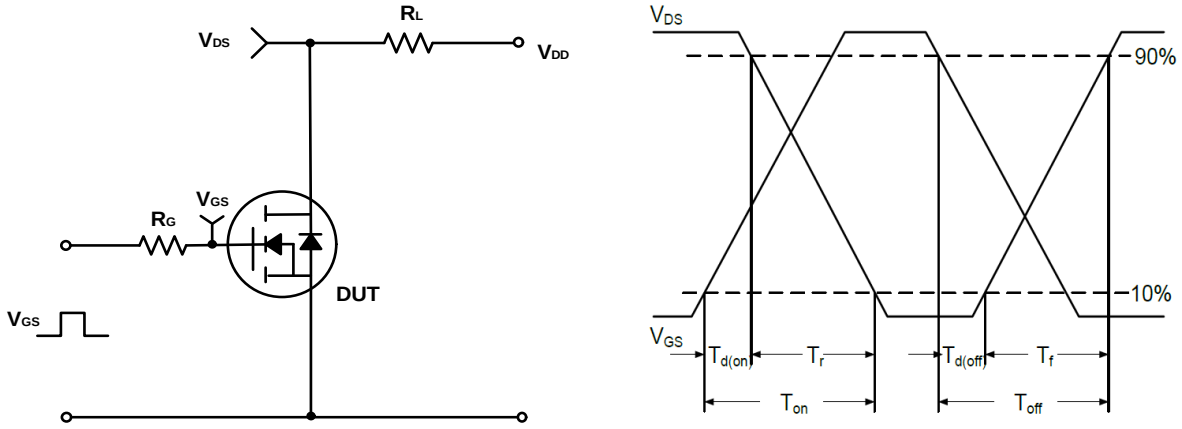



**Figure B. Switching Test Circuit & Waveforms**

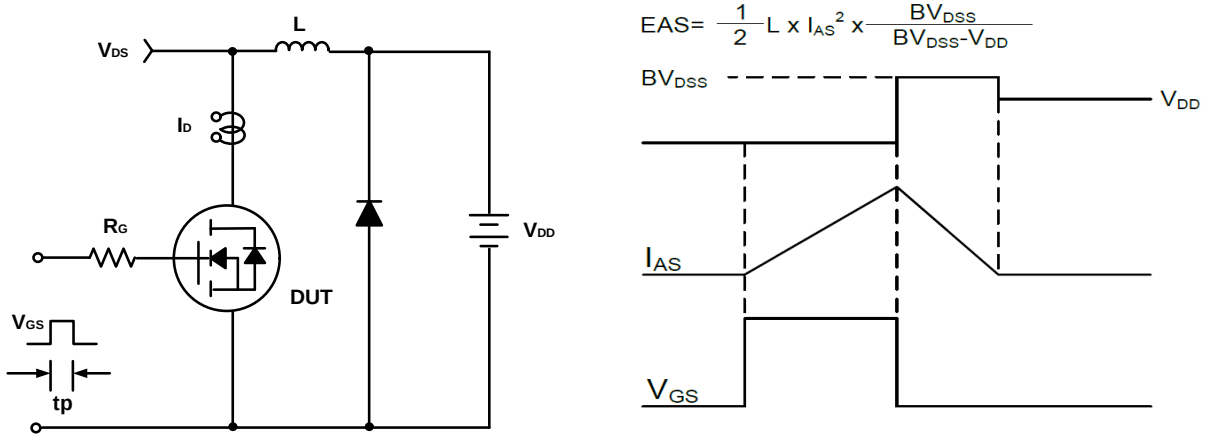
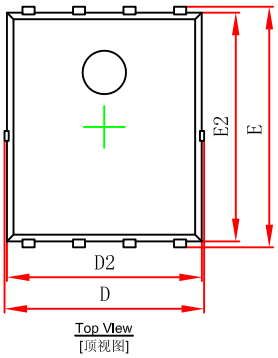
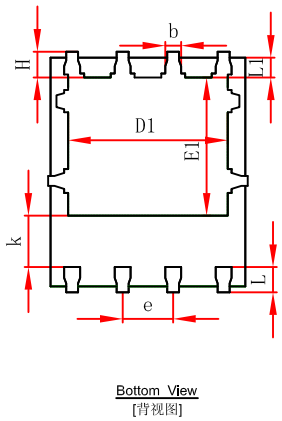
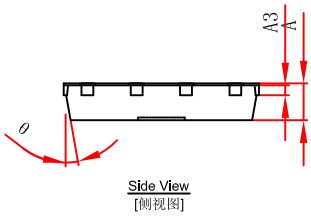



**Figure C. Unclamped Inductive Switching Circuit & Waveforms**

## PDFNWB5x6-8L Package Outline Dimensions

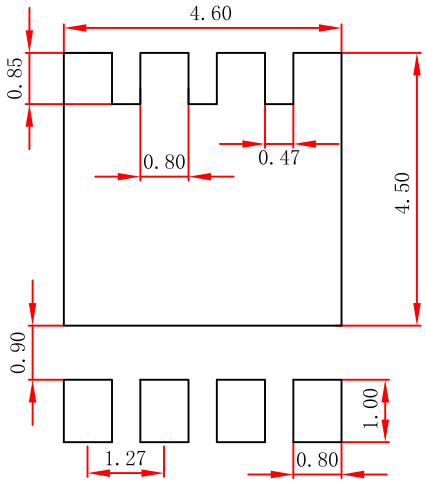



| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min. | Max. | Min. | Max. |
| A | 0.900 | 1.000 | 0.035 | 0.039 |
| A3 | 0.254REF. | | 0.010REF. | |
| D | 4.944 | 5.096 | 0.195 | 0.201 |
| E | 5.974 | 6.126 | 0.235 | 0.241 |
| D1 | 3.910 | 4.110 | 0.154 | 0.162 |
| E1 | 3.375 | 3.575 | 0.133 | 0.141 |
| D2 | 4.824 | 4.976 | 0.190 | 0.196 |
| E2 | 5.674 | 5.826 | 0.223 | 0.229 |
| k | 1.190 | 1.390 | 0.047 | 0.055 |
| b | 0.350 | 0.450 | 0.014 | 0.018 |
| e | 1.270TYP. | | 0.050TYP. | |
| L | 0.559 | 0.711 | 0.022 | 0.028 |
| L1 | 0.424 | 0.576 | 0.017 | 0.023 |
| H | 0.574 | 0.726 | 0.023 | 0.029 |
| θ | 10° | 12° | 10° | 12° |

## PDFNWB5x6-8L Suggested Pad Layout




Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.05mm.
3.The pad layout is for reference purposes only.