

General Description

The TF040N04NG combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. This device is ideal for load switch and battery protection applications.

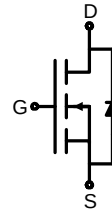
Features

- Advance high cell density Trench technology
- Low $R_{DS(ON)}$ to minimize conductive loss
- Low Gate Charge for fast switching
- Low Thermal resistance

Application

- MB/VGA Vcore
- SMPS 2nd Synchronous Rectifier
- POL application
- BLDC Motor driver

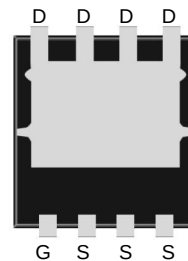
Product Summary



$$V_{DS} = 40V \quad I_D = 70A$$

$$R_{DS(ON)}(10V \text{ typ}) = 4.5m\Omega$$

$$R_{DS(ON)}(4.5V \text{ typ}) = 6.2m\Omega$$



PDFNWB5x6-8L

Ordering Information:

Part NO.	TF040N04NG
Marking 1	040N04NG:TF040N04NG
Marking 2	TF:tuofeng; AA:device code; Y:year code; X:Week
MOQ	5000

Absolute Maximum Ratings ($T_C = 25^\circ C$)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	$I_D @ T_C = 25^\circ C$	70	A
	$I_D @ T_C = 75^\circ C$	49	A
	$I_D @ T_C = 100^\circ C$	42	A
Pulsed Drain Current ①	I_{DM}	220	A
Total Power Dissipation	$P_D @ T_C = 25^\circ C$	42	W
Total Power Dissipation	$P_D @ T_A = 25^\circ C$	2.0	W
Operating Junction Temperature	T_J	-55 to 150	$^\circ C$
Storage Temperature	T_{STG}	-55 to 150	$^\circ C$

Note: ① Pulse Test : Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$;



Shenzhen Tuofeng Semiconductor Technology Co., Ltd

N-CHANNEL ENHANCEMENT MODE POWER MOSFET

SGT MOS、低内阻、低结电容开关损耗小

TF040N04NG

Single Pulse Avalanche Energy	E _{AS}	50			mJ	
Avalanche Current	I _{AS} I _{AR}	14			A	
●Thermal resistance						
Parameter	Symbol	Min.	Typ.	Max.	Unit	
Thermal resistance, junction - case	R _{thJC}	-	-	4.5	° C/W	
Thermal resistance, junction - ambient	R _{thJA}	-	-	60	° C/W	
Soldering temperature, wave soldering for 8s	T _{sold}	-	-	265	° C	
●Electronic Characteristics						
Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250uA	40			V
Gate Threshold Voltage	V _{GS(TH)}	V _{GS} =V _{DS} , I _D =250uA	1.2	1.9	2.5	V
Drain-Source Leakage Current	I _{DSS}	V _{DS} =40V, V _{GS} =0V			1.0	uA
Gate- Source Leakage Current	I _{GSS}	V _{GS} =±20V ,V _{DS} =0V			±100	nA
Static Drain-source On Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =20A		4.5	6.0	mΩ
		V _{GS} =4.5V, I _D =15A		6.2	8.5	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V, I _D =20A		78		S
Source-drain voltage	V _{SD}	IS=20A			1.20	V
●Electronic Characteristics						
Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Input capacitance	Ciss	Vds=20V,Vgs=0V f = 1MHz	-	1050	-	pF
Output capacitance	Coss		-	450	-	
Reverse transfer capacitance	Crss		-	15.0	-	
●Gate Charge characteristics(T _a = 25°C)						
Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Gate Risistance	R _g	f = 1MHz		3.9		Ω
Total gate charge	Qg	V _{DD} = 20V I _D = 20A V _{GS} = 10V	-	20.0	-	nC
Gate - Source charge	Qgs		-	3.50	-	
Gate - Drain charge	Qgd		-	4.40	-	
Turn-ON Delay time	t _{D(on)}	V _{GS} =10V ,V _{DS} =20V R _G =6.0Ω, I=20A		5.00		ns
Turn-ON Rise time	t _r			8.80		ns
Turn-Off Delay time	t _{D(off)}			24.0		ns
Turn-Off Fall time	t _f			15.5		ns

Fig.1 Power Dissipation

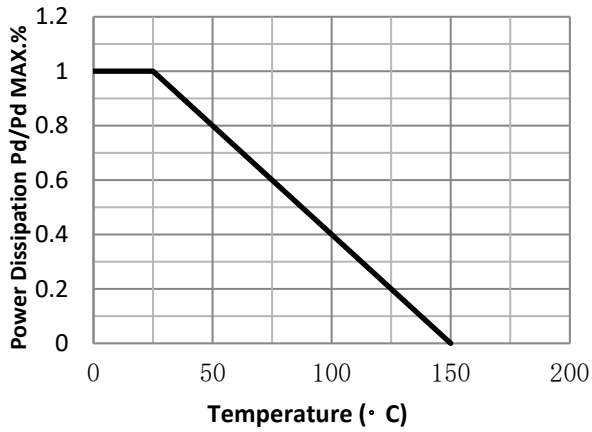


Fig.2 Typical output Characteristics

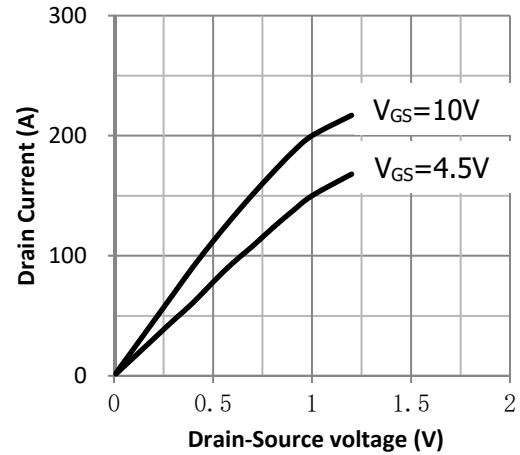


Fig.3 Threshold Voltage V.S Junction Temperature

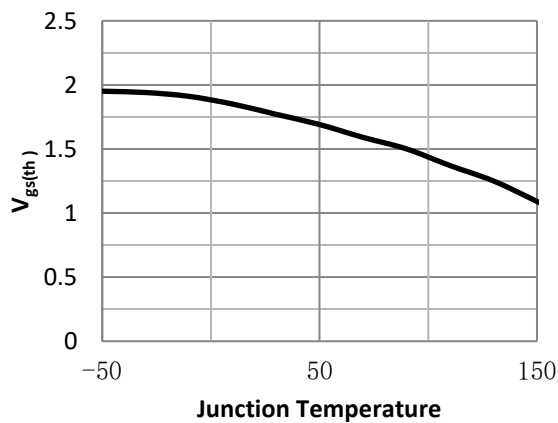


Fig.4 Resistance V.S Drain Current

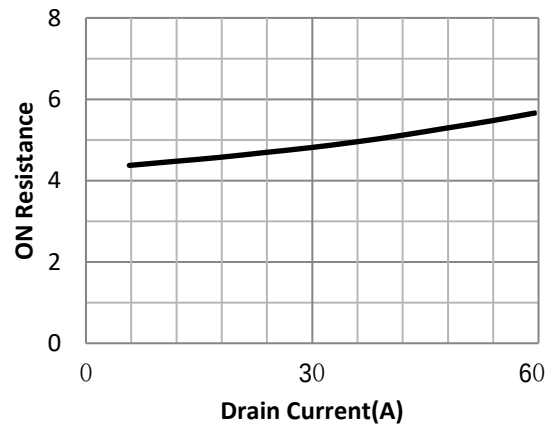


Fig.5 On-Resistance VS Gate Source Voltage

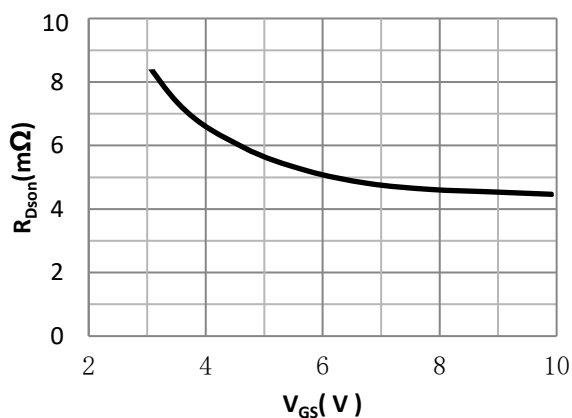


Fig.6 On-Resistance V.S Junction Temperature

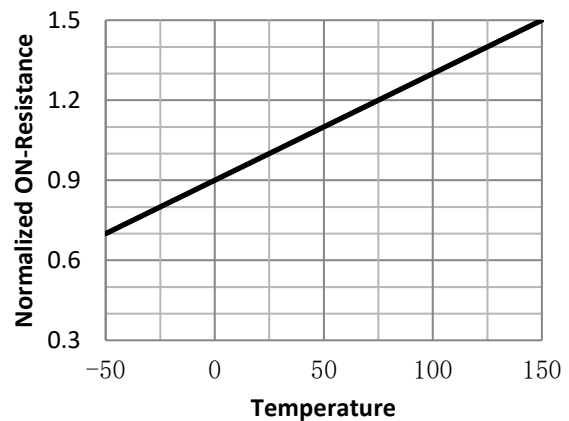


Fig.7 Switching Time Measurement Circuit

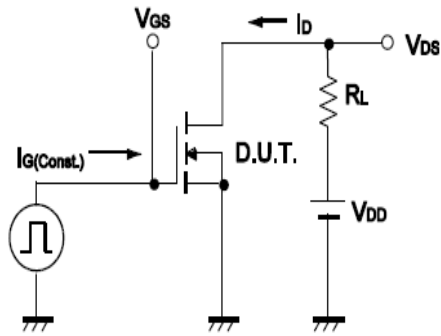


Fig.8 Gate Charge Waveform

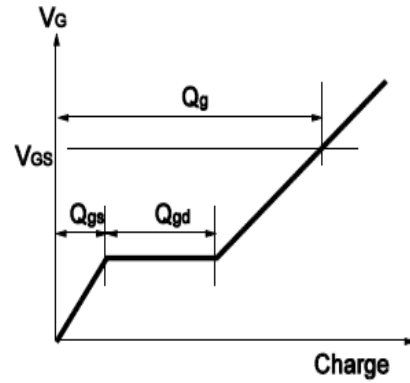


Fig.9 Switching Time Measurement Circuit

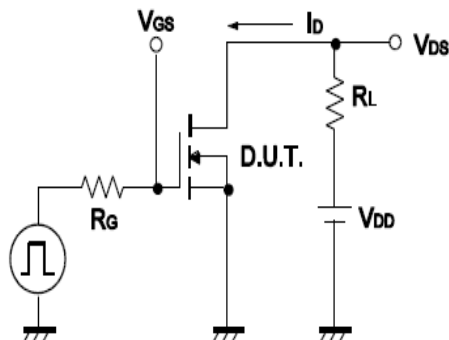


Fig.10 Gate Charge Waveform

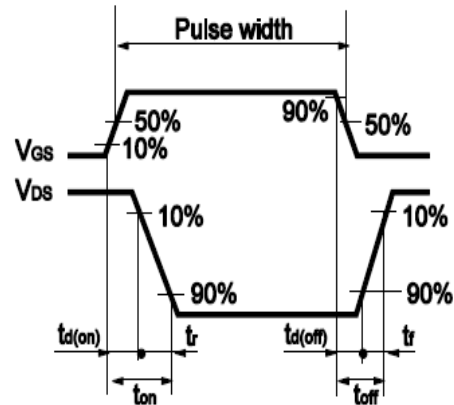


Fig.11 Avalanche Measurement Circuit

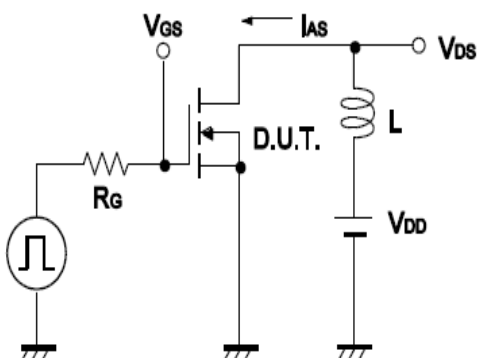
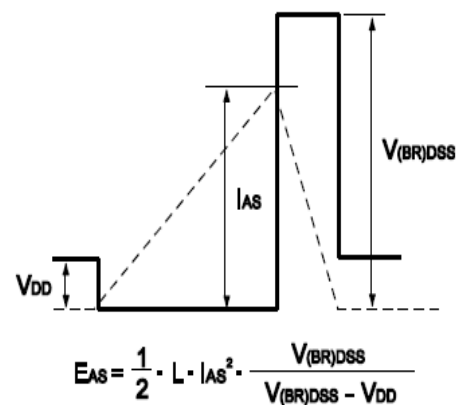
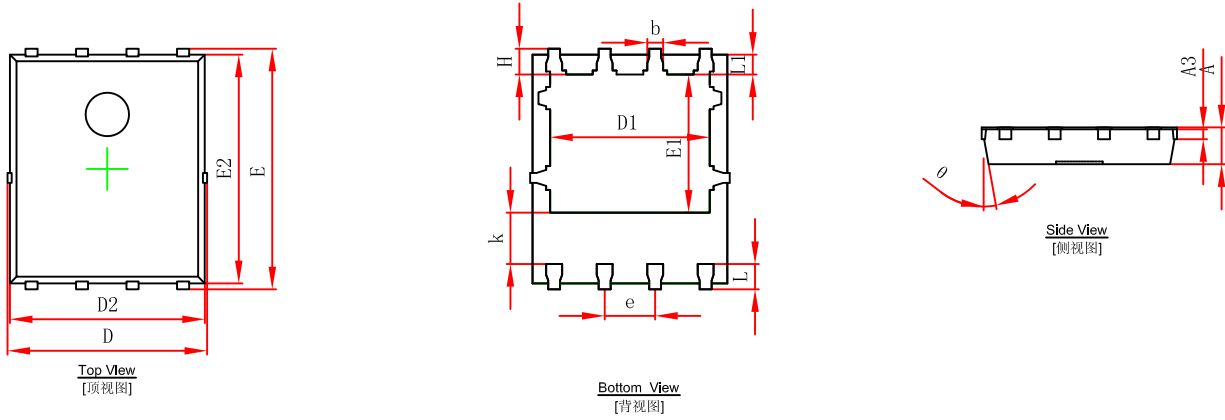


Fig.12 Avalanche Waveform

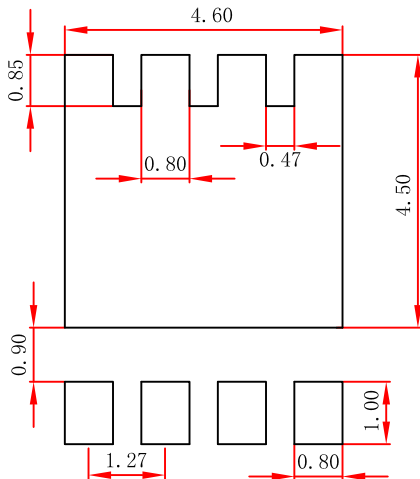


PDFNWB5x6-8L Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	10°	12°	10°	12°

PDFNWB5x6-8L Suggested Pad Layout



- Note:
1. Controlling dimension: in millimeters.
 2. General tolerance: $\pm 0.05\text{mm}$.
 3. The pad layout is for reference purposes only.