N-CHANNEL ENHANCEMENT MODE POWER MOSFET

SGT MOS、低内阻、低结电容开关损耗小

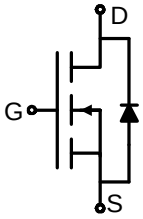
TF090N15NG

Description

TF090N15NG uses advanced power trench MOSFET technology that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance. This device is well suited for high efficiency fast switching applications.

RoHS compliant

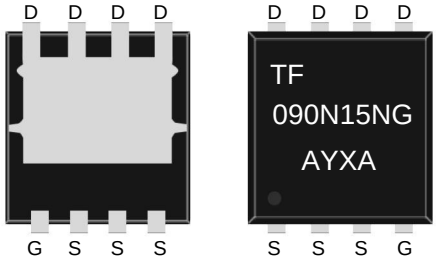
Product Summary



V_{DS}=150V I_D=75A

$R_{DS(10V\ TYP)}$ = 8.8mΩ

$R_{DS(4.5V\ TYP)}$ =10.0mΩ



PDFNWB5x6-8L

Applications

- DC/DC Converter
- Power Management Switches

Package Marking and Ordering Information:

Part NO.	TF090N15NG
Marking1	090N15NG:TF090N15NG
Marking2	TF:tuofeng; Y:year code; X:Week; AA:device code;
Basic ordering unit (pcs)	5000

Absolute Maximum Ratings（T_A = 25°C, unless otherwise noted）

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	150	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C=25°C	I_D	75	A
	T_C=100°C		45	
Pulsed Drain Current[1]		I_{DM}	300	A
Single Pulse Avalanche Energy[2]		EAS	115	mJ
Total Power Dissipation	T_C=25°C	P_D	125	W
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance from Junction-to-Ambient[3]	$R_{\theta JA}$	54	°C/W
Thermal Resistance from Junction-to-Case	$R_{\theta JC}$	1.0	°C/W

Electrical Characteristics（T_J = 25°C, unless otherwise noted）

Parameter		Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics							
Drain-Source Breakdown Voltage		$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	150	-	-	V
Gate-body Leakage current		I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V	-	-	±100	nA
Zero Gate Voltage Drain Current	T_J=25°C	I_{DSS}	V_{DS} =150V, V_{GS} = 0V	-	-	1	μA
	T_J=100°C			-	-	100	
Gate-Threshold Voltage		$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	1.5	2.0	2.5	V
Drain-Source on-Resistance[4]		$R_{DS(on)}$	V_{GS} = 10V, I_D = 20A	-	8.8	12	mΩ
			V_{GS} = 4.5V, I_D = 15A	-	10	14	
Forward Transconductance[4]		g_{fs}	V_{DS} = 10V, I_D = 20A	-	85	-	S
Dynamic Characteristics[5]							
Input Capacitance		C_{iss}	V_{DS} = 50V, V_{GS} =0V, f =1MHz	-	3450	-	pF
Output Capacitance		C_{oss}		-	268	-	
Reverse Transfer Capacitance		C_{rss}		-	9.4	-	
Gate Resistance		R_g	f =1MHz	-	1.3	-	Ω
Switching Characteristics[5]							
Total Gate Charge		Q_g	V_{GS} = 10V, V_{DS} = 50V, I_D=20A	-	111.2	-	nC
Gate-Source Charge		Q_{gs}		-	17.5	-	
Gate-Drain Charge		Q_{gd}		-	30.2	-	
Turn-on Delay Time		$t_{d(on)}$	V_{GS} =10V, V_{DD} =50V, R_G = 3Ω, I_D= 20A	-	22.2	-	ns
Rise Time		t_r		-	37.8	-	
Turn-off Delay Time		$t_{d(off)}$		-	95.2	-	
Fall Time		t_f		-	35.6	-	
Body Diode Reverse Recovery Time		t_{rr}	I_F = 20A, dI/dt=100A/μs	-	59.4	-	ns
Body Diode Reverse Recovery Charge		Q_{rr}		-	91.8	-	nC
Drain-Source Body Diode Characteristics							
Diode Forward Voltage[4]		V_{SD}	I_S = 20A, V_{GS} = 0V	-	-	1.2	V
Continuous Source Current	T_C=25°C	I_S	-	-	-	120	A

Notes:

1. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C.
2. The EAS data shows Max. rating . The test condition is V_{DD}=50V, V_{GS}=10V, L=0.4mH, I_{AS}=24A
3. The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper,The value in any given application depends on the user's specific board design.
4. The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%.
5. This value is guaranteed by design hence it is not included in the production test.

Typical Characteristics

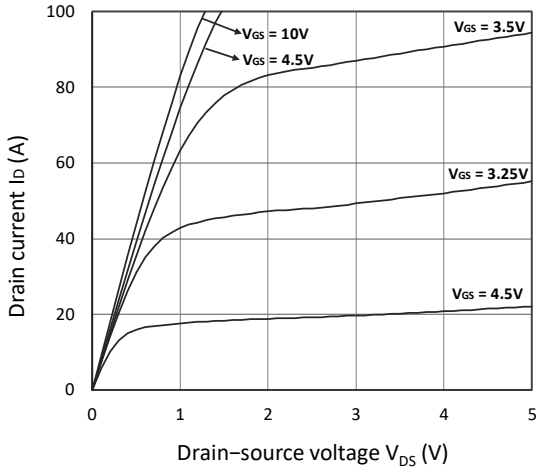


Figure 1. Output Characteristics

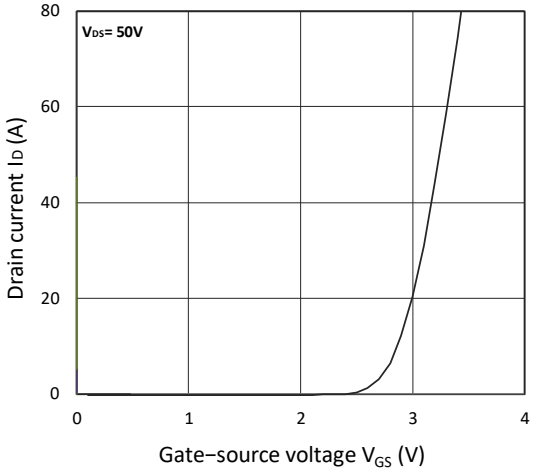


Figure 2. Transfer Characteristics

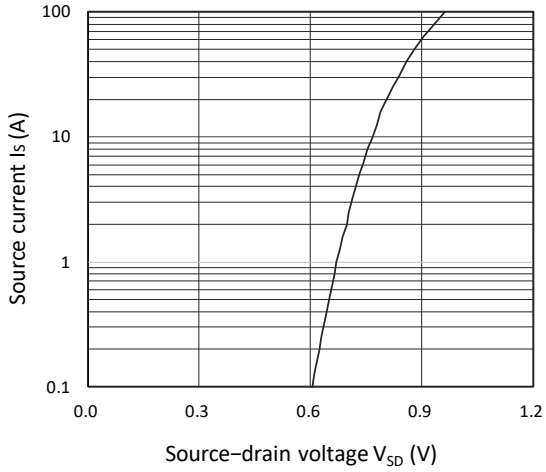


Figure 3. Forward Characteristics of Reverse

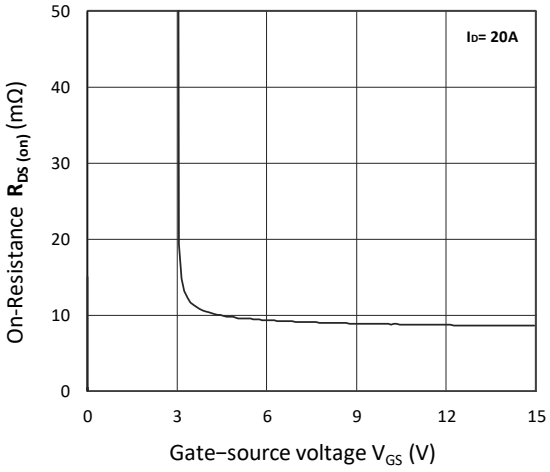


Figure 4. $R_{DS(ON)}$ vs. V_{GS}

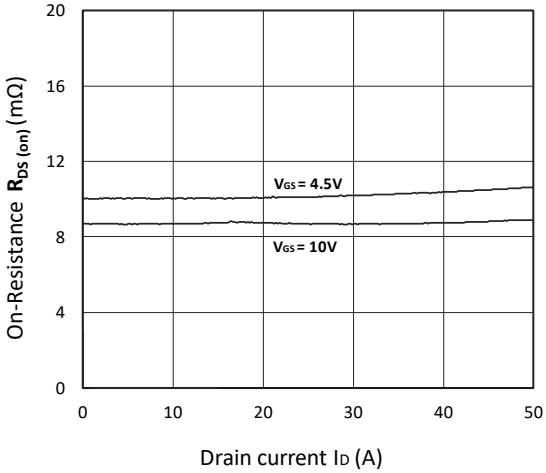


Figure 5. $R_{DS(ON)}$ vs. I_D

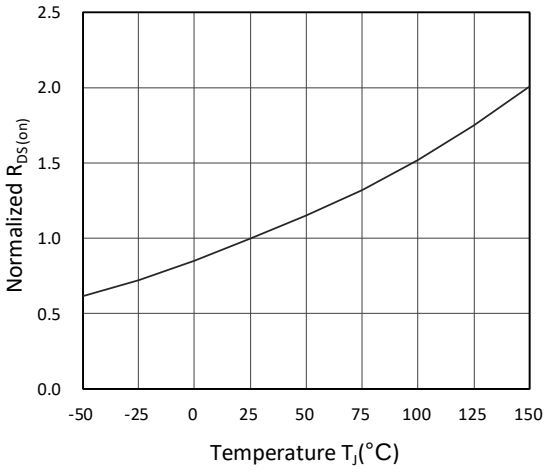


Figure 6. Normalized $R_{DS(on)}$ vs. Temperature

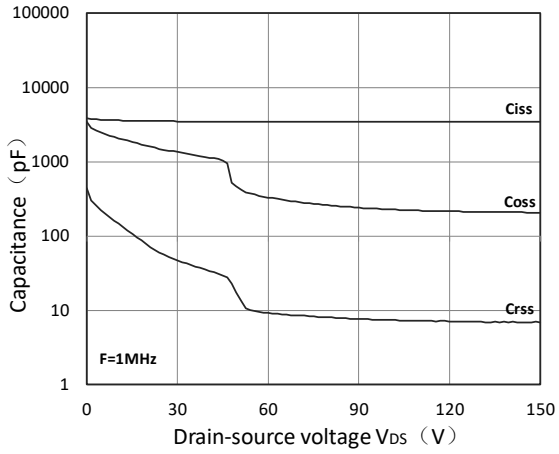


Figure 7. Capacitance Characteristics

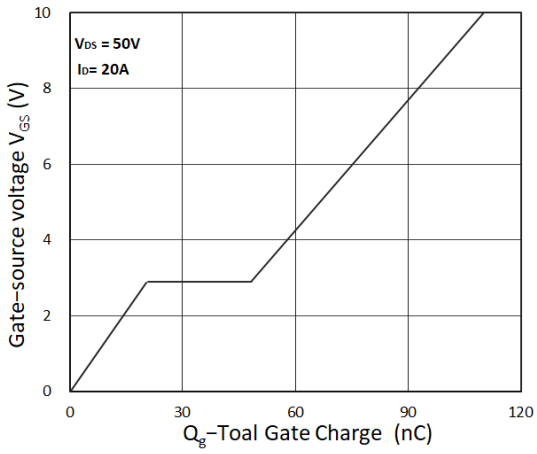


Figure 8. Gate Charge Characteristics

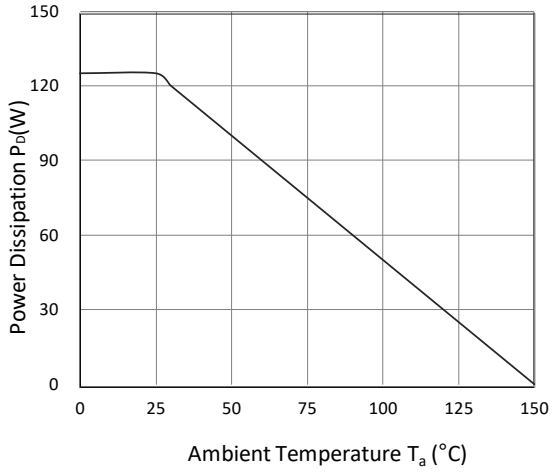


Figure 9. Power Dissipation

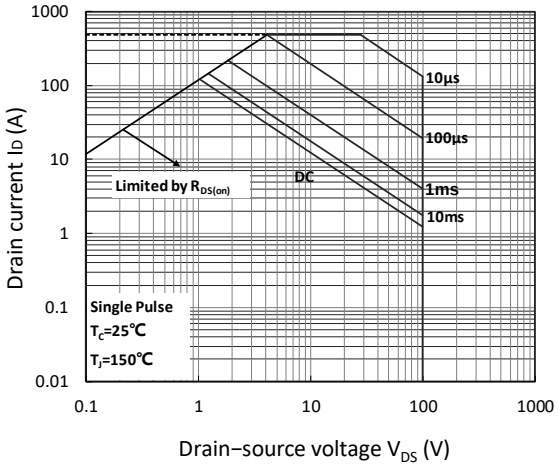


Figure10. Safe Operating Area

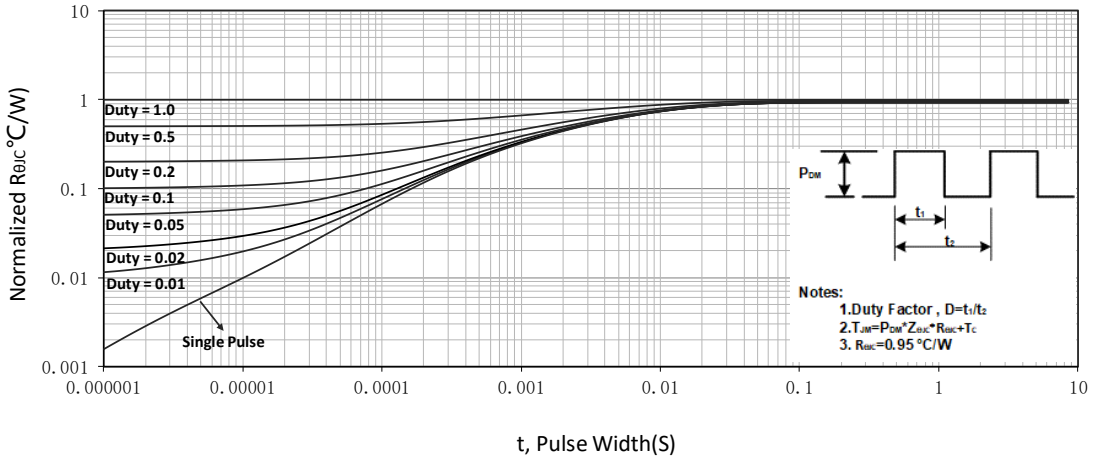


Figure 11. Normalized Maximum Transient Thermal Impedance

Test Circuit

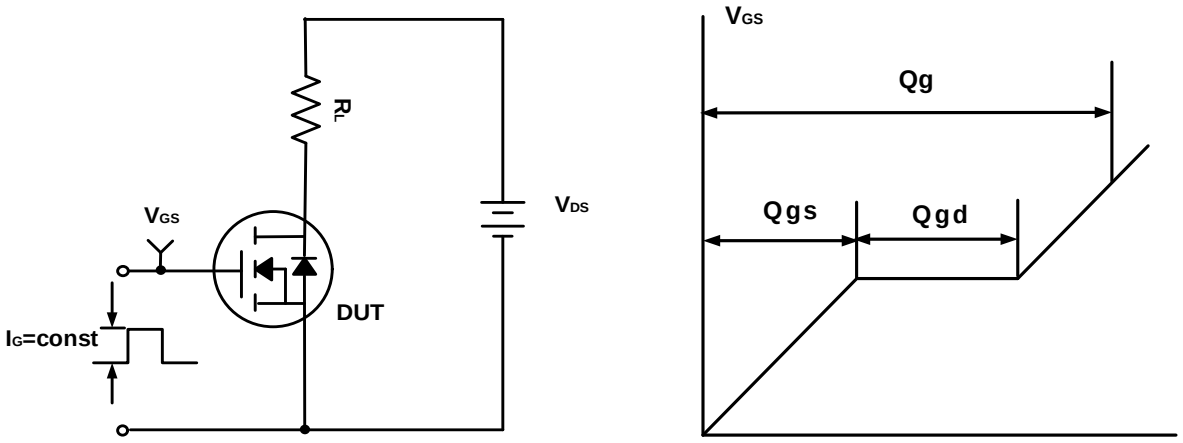


Figure A. Gate Charge Test Circuit & Waveforms

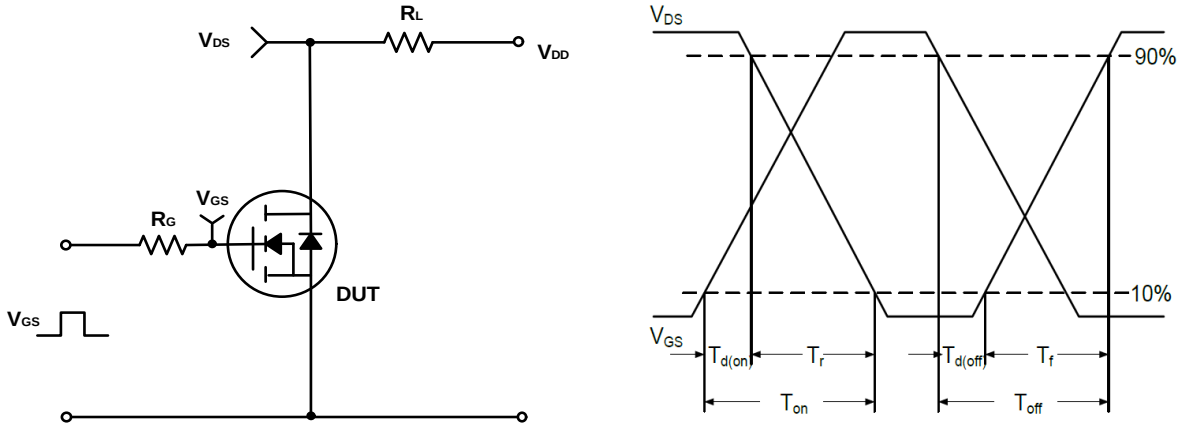


Figure B. Switching Test Circuit & Waveforms

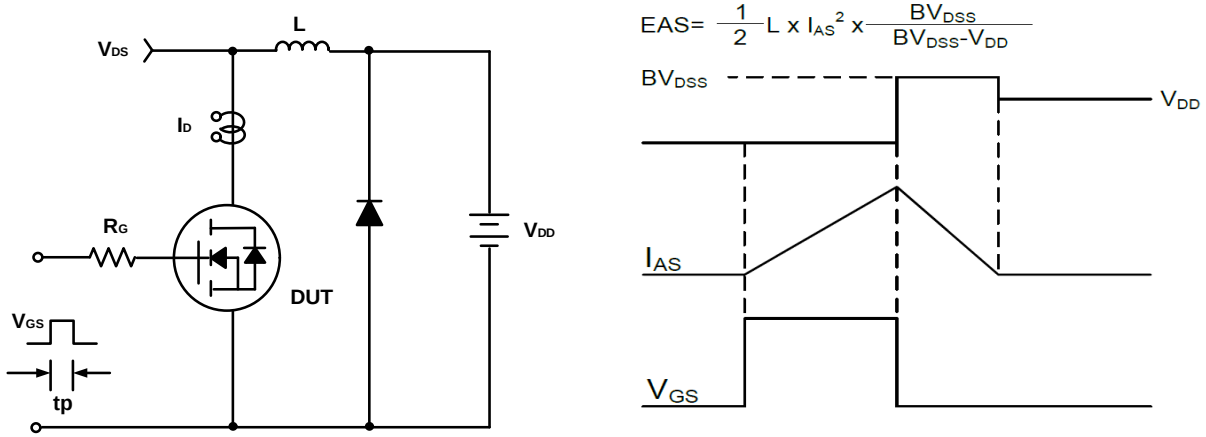
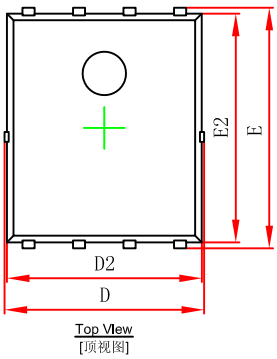
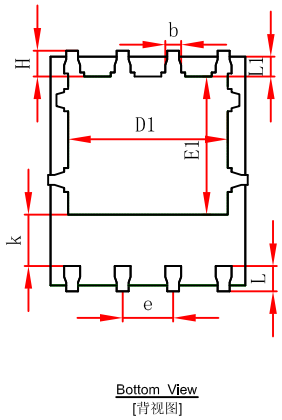
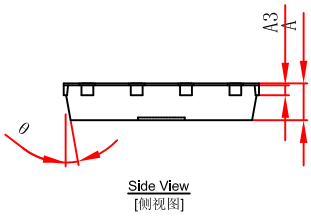


Figure C. Unclamped Inductive Switching Circuit & Waveforms

PDFNWB5x6-8L Package Outline Dimensions

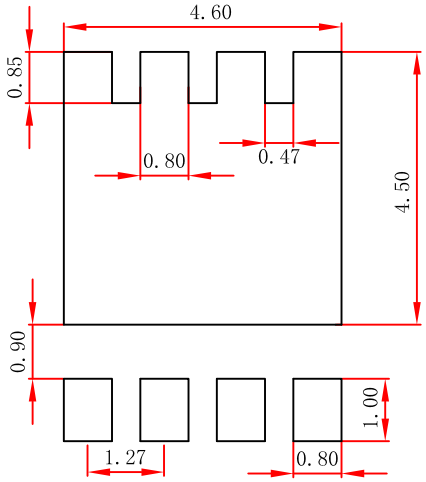






Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	10°	12°	10°	12°

PDFNWB5x6-8L Suggested Pad Layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.05mm.
3.The pad layout is for reference purposes only.