N-CHANNEL ENHANCEMENT MODE POWER MOSFET

SGT MOS、低内阻、低结电容开关损耗小 **TF030N06NG**

● General Description

The TF030N06NG uses advanced trench technology and design to provide excellent RDS(ON) withlowgate charge. It can be used in a wide variety ofapplications.

● Features

Advance device constructure

Low $R_{DS(ON)}$ to minimize conduction loss

Low Gate Charge for fast switching

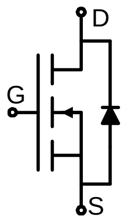
Low Thermal resistance

●Application

Synchronous Rectification for AC-DC/DC-DC converter

Power Tools

● Product Summary

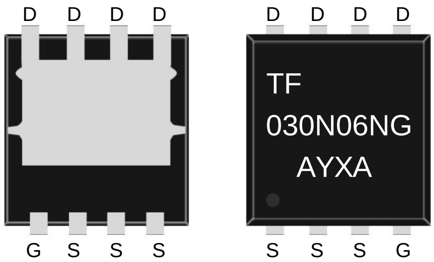


V_{DS} =60V I_D=110A

$R_{DSON(10V\ typ)}$ =3.3mΩ

$R_{DSON(4.5V\ typ)}$ =4.8mΩ

RoHS compliant



PDFNWB5x6-8L

●Package Marking and Ordering Information:

Part NO.	TF030N06NG
Marking1	030N06NG
Marking2	TF:tuofeng; AA:device code; Y:year code; X:Week
MOQ	5000

●Absolute Maximum Ratings (Tc =25℃)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current	$I_{D@}$TC=25℃	110	A
	$I_{D@}$TC=75℃	77	A
	$I_{D@}$TC=100℃	66	A
Pulsed Drain Current ①	I_{DM}	288	A
Total Power Dissipation	P_D@TC=25℃	55	W
Total Power Dissipation	P_D@TA=25℃	2.0	W
Operating Junction Temperature	T_J	-55 to 150	℃
Storage Temperature	T_{STG}	-55 to 150	℃
Single Pulse Avalanche Energy	E_{AS}	80	mJ

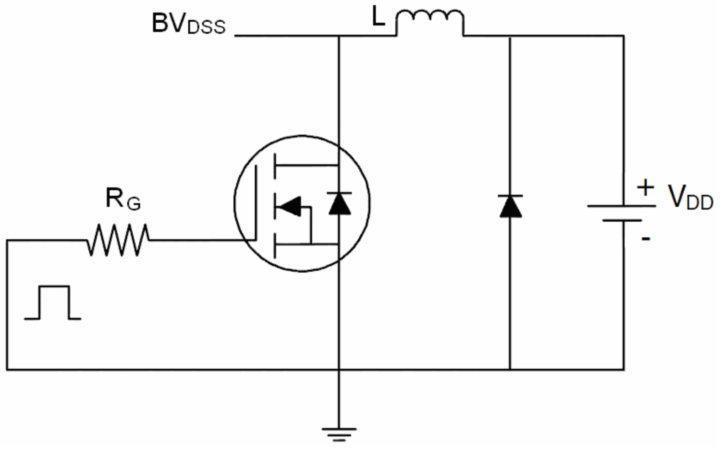
Electrical Characteristics (T_J = 25°C, unless otherwise noted)

Parameter		Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics							
Drain-Source Breakdown Voltage		$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	60	-	-	V
Gate-body Leakage Current		I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V	-	-	±100	nA
Zero Gate Voltage Drain Current	T_J=25°C	I_{DSS}	V_{DS} = 58V, V_{GS} = 0V	-	-	1	μA
	T_J=100°C			-	-	100	
Gate-Threshold Voltage		$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	1.2	1.9	2.5	V
Drain-Source On-Resistance[4]		$R_{DS(on)}$	V_{GS} = 10V, I_D = 20A	-	3.3	5.0	mΩ
			V_{GS} = 4.5V, I_D = 15A	-	4.8	6.7	
Forward Transconductance[4]		g_{fs}	V_{DS} = 10V, I_D = 20A	-	89	-	S
Dynamic Characteristics[5]							
Input Capacitance		C_{iss}	V_{DS} = 30V, V_{GS} =0V, f =1MHz	-	1990	-	pF
Output Capacitance		C_{oss}		-	735	-	
Reverse Transfer Capacitance		C_{rss}		-	42	-	
Gate Resistance		R_g	f = 1MHz	-	1.8	-	Ω
Switching Characteristics[5]							
Total Gate Charge		Q_g	V_{GS} = 10V, V_{DS} = 30V, I_D= 20A	-	35	-	nC
Gate-Source Charge		Q_{gs}		-	6.6	-	
Gate-Drain Charge		Q_{gd}		-	8.4	-	
Turn-On Delay Time		$t_{d(on)}$	V_{GS} =10V, V_{DD} = 30V, R_G = 3Ω, I_D= 20A	-	9.4	-	ns
Rise Time		t_r		-	8.4	-	
Turn-Off Delay Time		$t_{d(off)}$		-	32.5	-	
Fall Time		t_f		-	12.5	-	
Body Diode Reverse Recovery Time		t_{rr}	I_F=20A, dI/dt=100A/μs	-	50	-	ns
Body Diode Reverse Recovery Charge		Q_{rr}		-	20	-	nC
Drain-Source Body Diode Characteristics							
Diode Forward Voltage[4]		V_{SD}	I_S = 20A, V_{GS} = 0V	-	-	1.2	V
Continuous Source Current	T_C=25°C	I_S	-	-	-	72	A

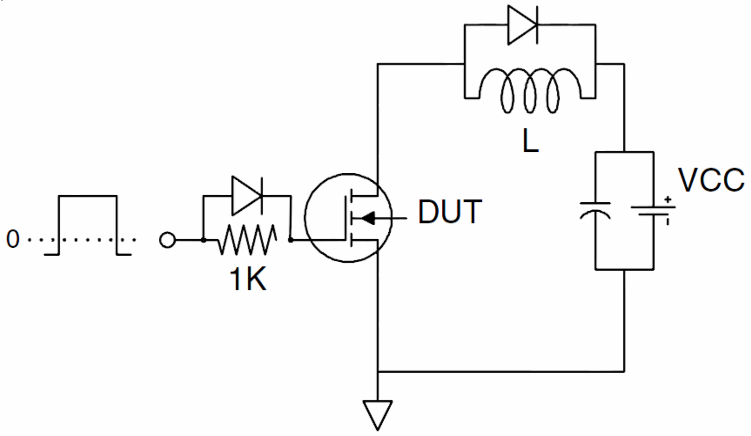
Notes:
1. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C
2. The EAS data shows Max. rating . The test condition is V_{DD}=25V,V_{GS}=10V,L=0.1mH，I_{AS}=40A.
3. The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%.
5. This value is guaranteed by design hence it is not included in the production test.

Test Circuit

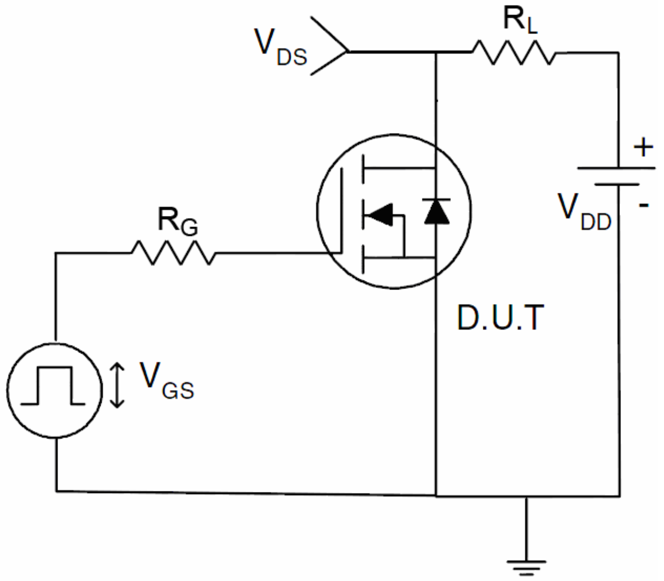
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Characteristics

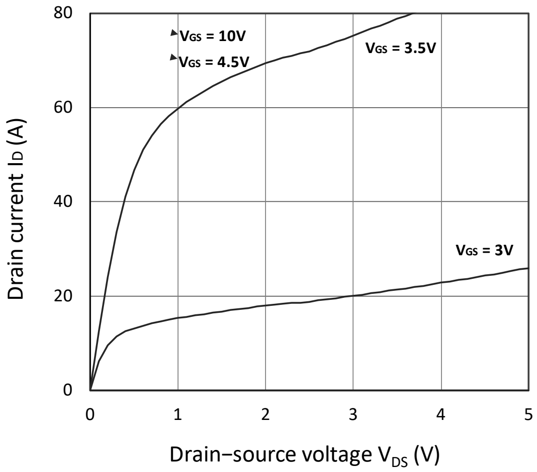


Figure 1. Output Characteristics

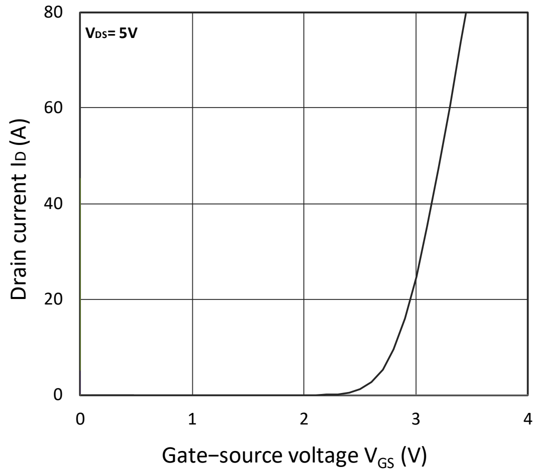


Figure 2. Transfer Characteristics

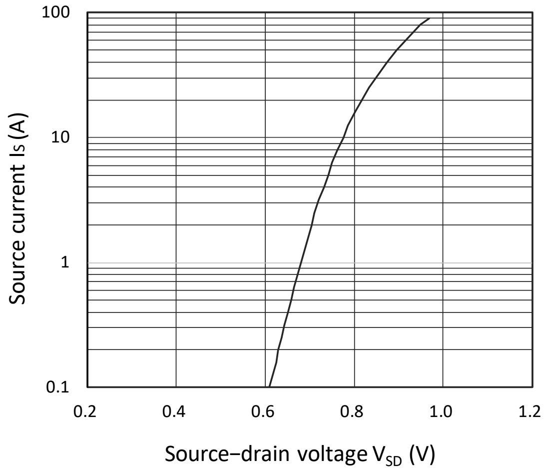


Figure 3. Forward Characteristics of Reverse

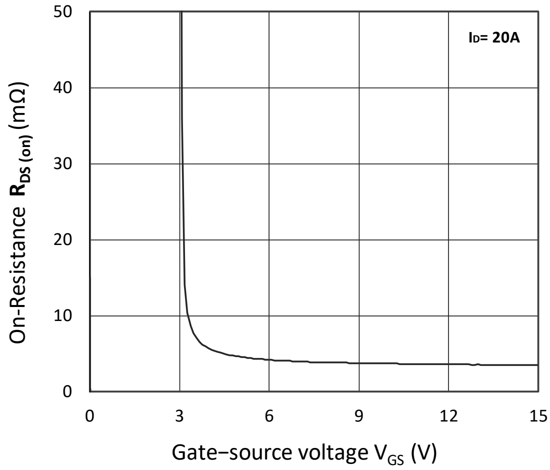


Figure 4. $R_{DS(ON)}$ vs. V_{GS}

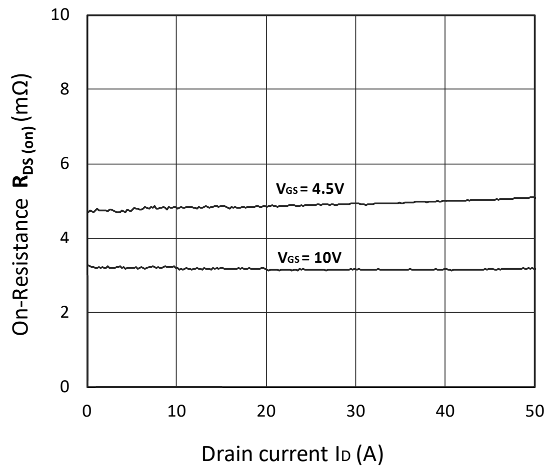


Figure 5. $R_{DS(ON)}$ vs. I_D

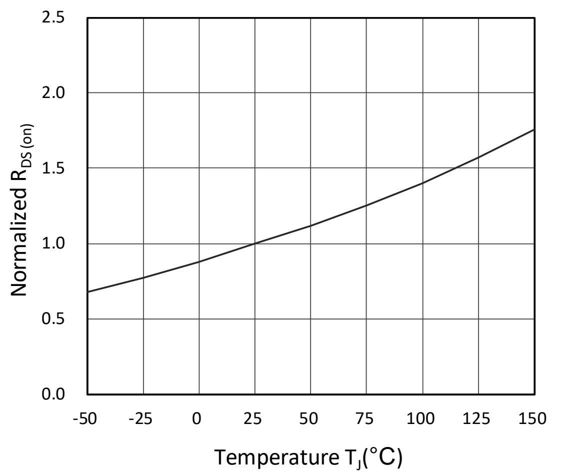


Figure 6. Normalized $R_{DS(on)}$ vs. Temperature

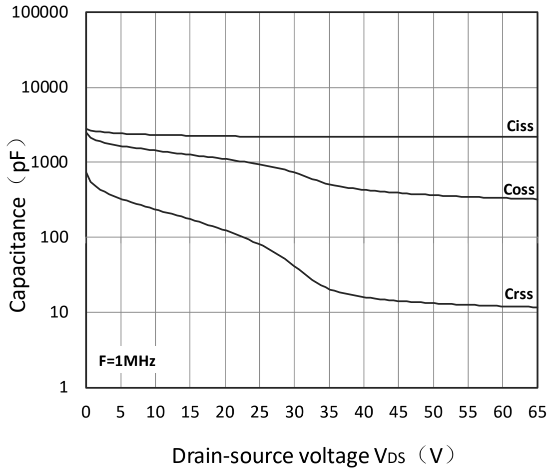


Figure 7. Capacitance Characteristics

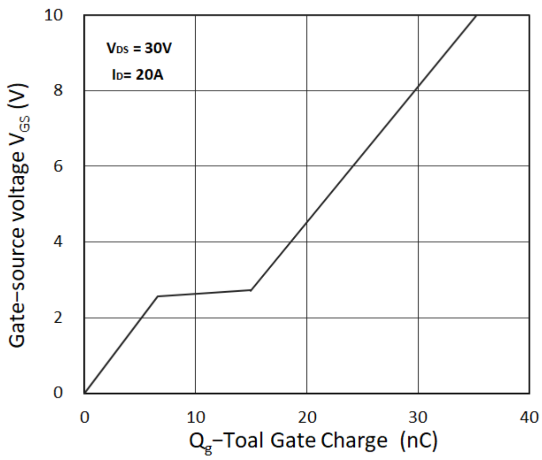


Figure 8. Gate Charge Characteristics

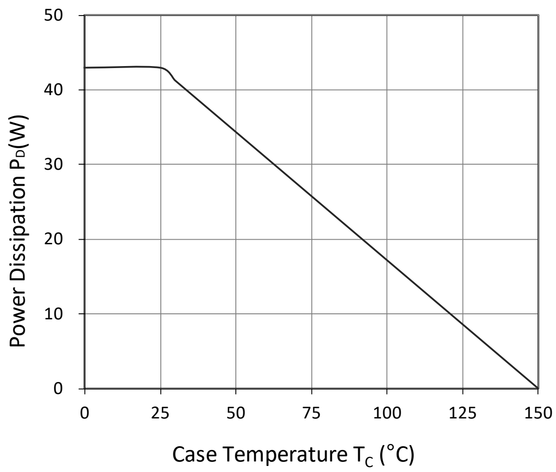


Figure 9. Power Dissipation

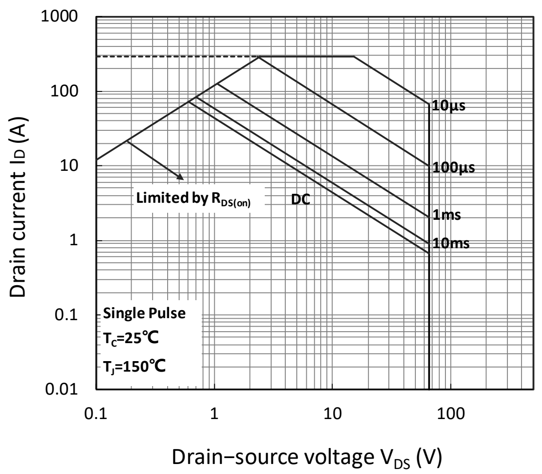


Figure10. Safe Operating Area

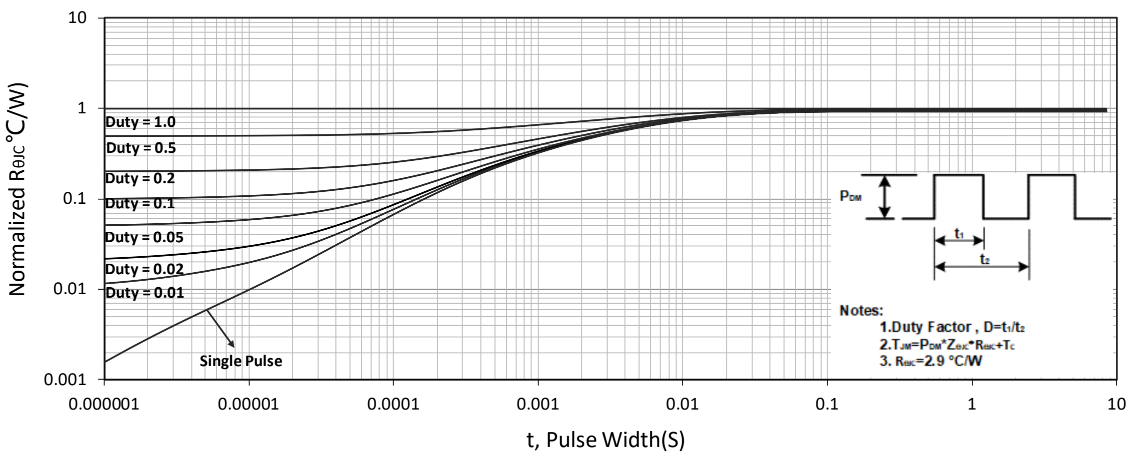
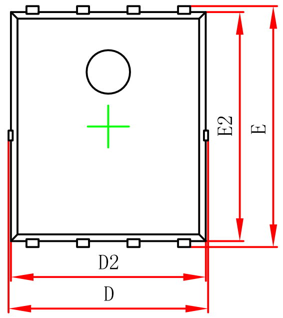
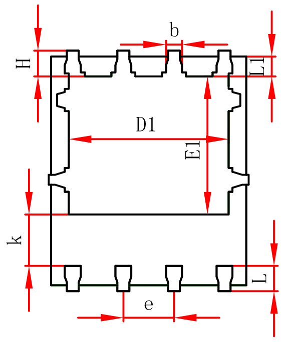


Figure 11. Normalized Maximum Transient Thermal Impedance

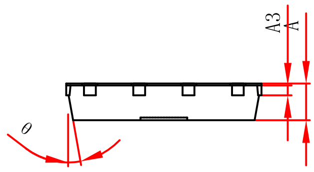
PDFNWB5x6-8L Package Outline Dimensions



Top View
[顶视图]



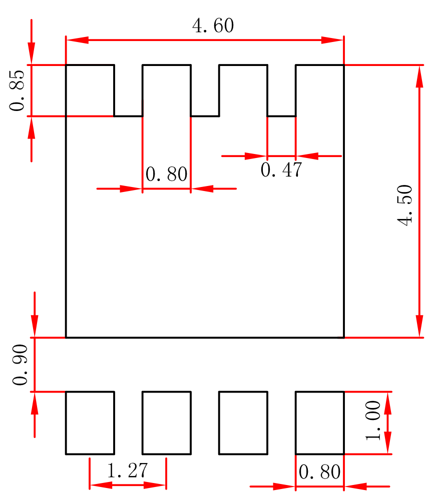
Bottom View
[背视图]



Side View
[侧视图]

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	10°	12°	10°	12°

PDFNWB5x6-8L Suggested Pad Layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.05mm.
3.The pad layout is for reference purposes only.