Shenzhen Tuofeng Semiconductor Technology Co., Ltd

N-CHANNEL ENHANCEMENT MODE POWER MOSFET

TF120N10DG

Features

- Vds = 100V , Id =120A
  $R_{DS(ON)}$=3.4mΩ (typ.) @ V_{GS}=10V
  $R_{DS(ON)}$=4.9mΩ (typ.) @ V_{GS}=4.5V
- Low $R_{DS(ON)}$
- Good stability and uniformity with high EAS High Current Capability
- Excellent package for good heat dissipation
- Fully characterized avalanche voltage and current

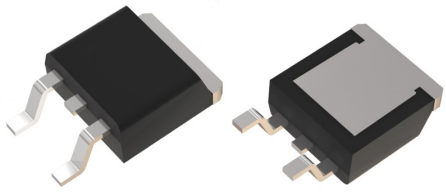
Application

- Power management
- Hard switched and high frequency circuits
- Uninterruptible power supply

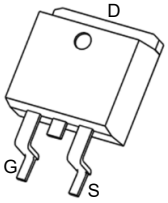
RoHS compliant

Package

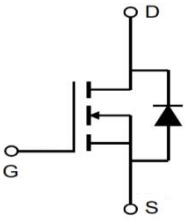
Top View



Top View



Schematic diagram



Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
TF120N10DG	TF120N10DG	TO-263	-	-	-

Absolute Maximum Ratings (T_C=25℃ unless otherwise specified)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C=25°C	I_D	120	A
	T_C=100°C		72	
Pulsed Drain Current[1]		I_{DM}	480	A
Single Pulse Avalanche Energy[2]		EAS	300	mJ
Total Power Dissipation	T_C=25°C	P_D	200	W
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C
Thermal Resistance from Junction-to-Ambient[3]		$R_{\theta JA}$	35	°C/W
Thermal Resistance from Junction-to-Case		$R_{\theta JC}$	0.5	°C/W

Electrical Characteristics (T_J = 25°C, unless otherwise noted)

Parameter		Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics							
Drain-Source Breakdown Voltage		$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	100	-	-	V
Gate-body Leakage current		I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V	-	-	±100	nA
Zero Gate Voltage Drain Current	T_J=25°C	I_{DSS}	V_{DS} = 90V, V_{GS} = 0V	-	-	1	μA
	T_J=100°C			-	-	100	
Gate-Threshold Voltage		$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	1.2	1.7	2.5	V
Drain-Source on-Resistance[4]		$R_{DS(on)}$	V_{GS} = 10V, I_D = 20A	-	3.4	4.2	mΩ
			V_{GS} = 4.5V, I_D =20A	-	4.9	6.0	
Dynamic Characteristics[5]							
Input Capacitance		C_{iss}	V_{DS} = 50V, V_{GS} =0V, f =1MHz	-	6095	-	pF
Output Capacitance		C_{oss}		-	722	-	
Reverse Transfer Capacitance		C_{rss}		-	17	-	
Gate Resistance		R_g	f=1MHz	-	1.3	-	Ω
Switching Characteristics[5]							
Total Gate Charge		Q_g	V_{GS} = 10V, V_{DS} = 50V, I_D= 20A	-	111.2	-	nC
Gate-Source Charge		Q_{gs}		-	17.5	-	
Gate-Drain Charge		Q_{gd}		-	30.2	-	
Turn-on Delay Time		$t_{d(on)}$	V_{GS} =10V, V_{DD} = 50V, R_G = 3Ω, I_D= 20A	-	22.2	-	ns
Rise Time		t_r		-	37.8	-	
Turn-off Delay Time		$t_{d(off)}$		-	95.3	-	
Fall Time		t_f		-	35.6	-	
Body Diode Reverse Recovery Time		t_{rr}	I_F=20A, di/dt = 100A/μs	-	59.4	-	ns
Body Diode Reverse Recovery Charge		Q_{rr}		-	91.8	-	nC
Drain-Source Body Diode Characteristics							
Diode Forward Voltage[4]		V_{SD}	I_S = 20A, V_{GS} = 0V	-	-	1.2	V
Continuous Source Current	T_C=25°C	I_S	-	-	-	120	A

Notes:

1. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C.
2. The EAS data shows Max. rating . The test condition is V_{DD}=35V, V_{GS}=10V, L=0.4mH, I_{AS}=40A.
3. The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%.
5. This value is guaranteed by design hence it is not included in the production test.

Typical Characteristics

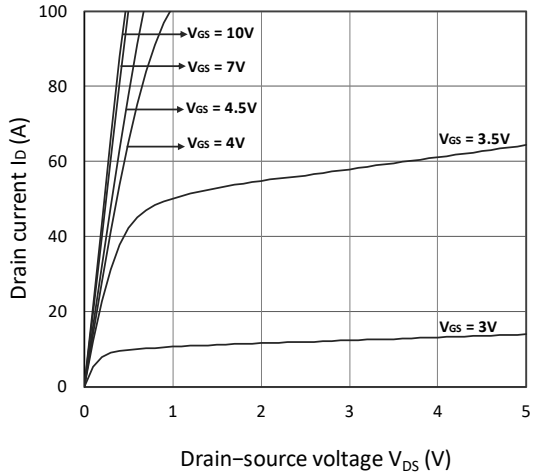


Figure 1. Output Characteristics

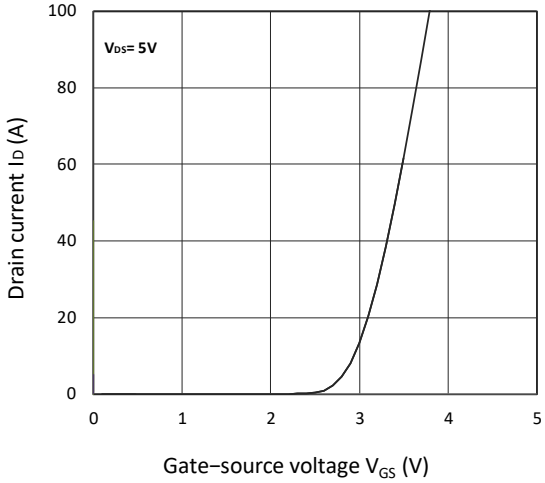


Figure 2. Transfer Characteristics

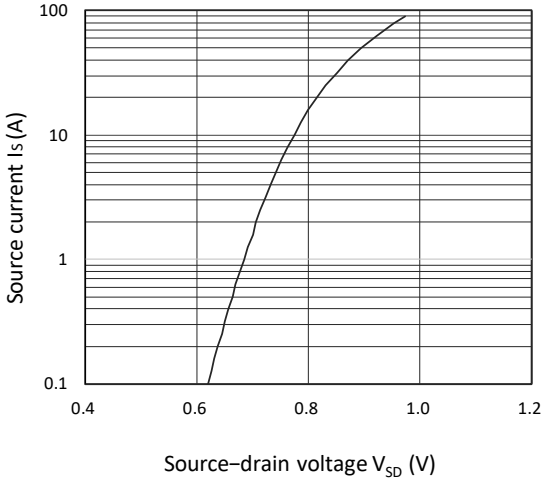


Figure 3. Forward Characteristics of Reverse

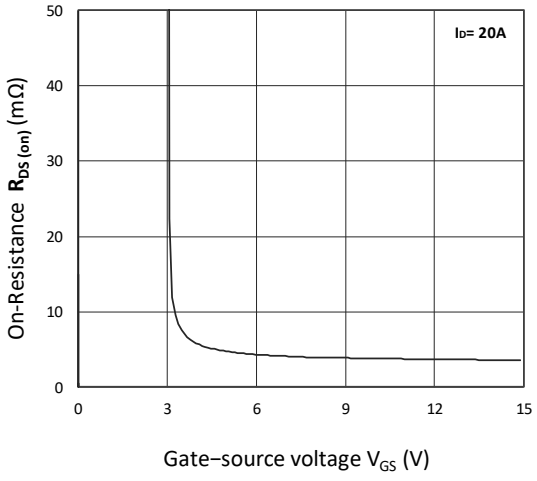


Figure 4. $R_{DS(ON)}$ vs. V_{GS}

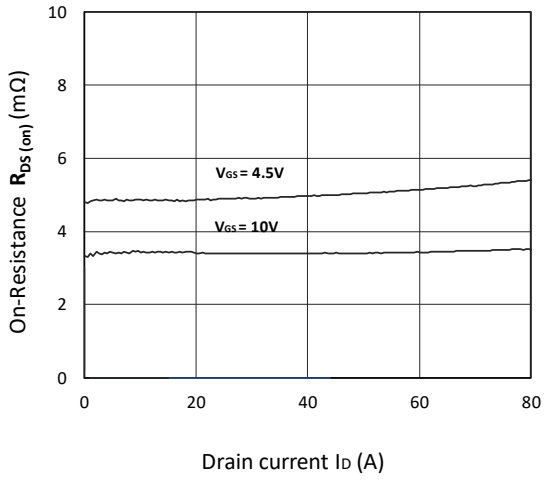


Figure 5. $R_{DS(ON)}$ vs. I_D

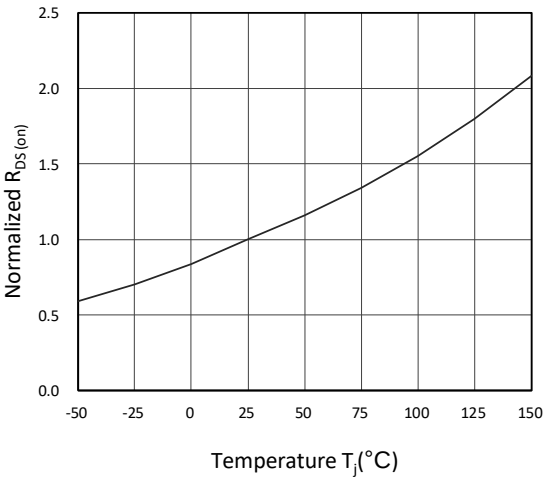


Figure 6. Normalized $R_{DS(on)}$ vs. Temperature

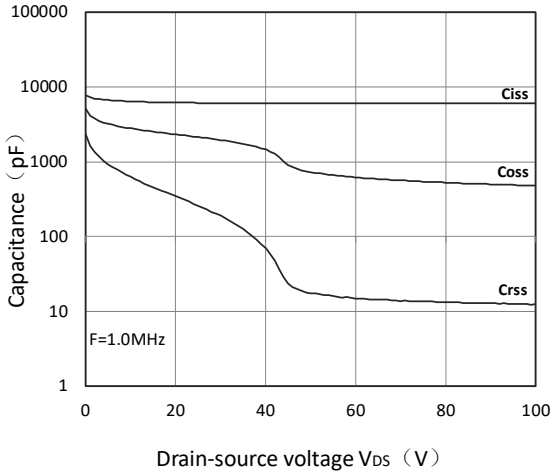


Figure 7. Capacitance Characteristics

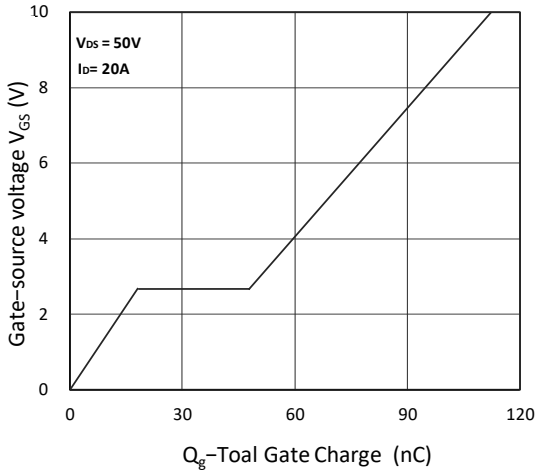


Figure 8. Gate Charge Characteristics

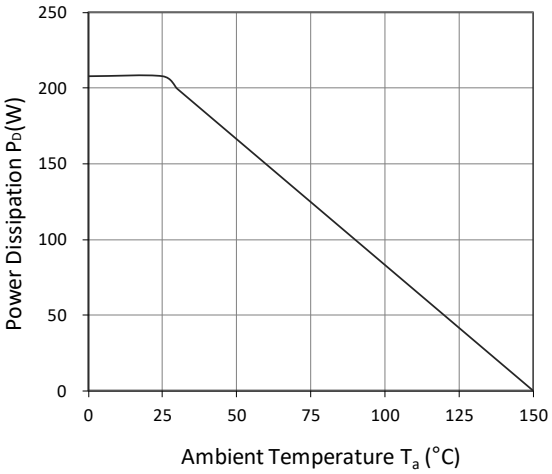


Figure 9. Power Dissipation

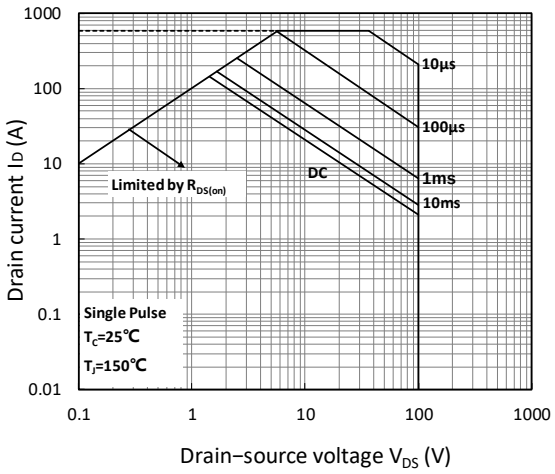


Figure10. Safe Operating Area

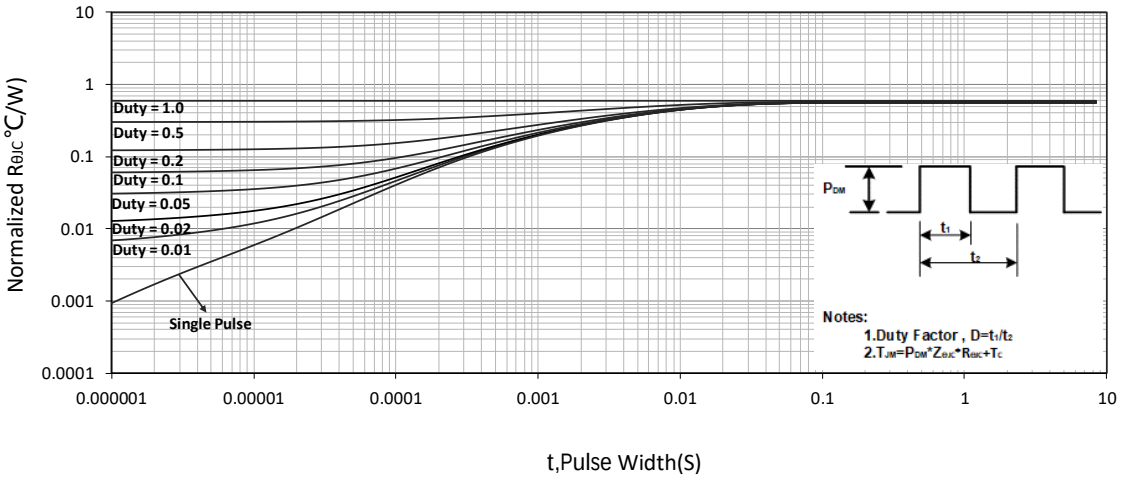


Figure 11. Normalized Maximum Transient Thermal Impedance

Test Circuit

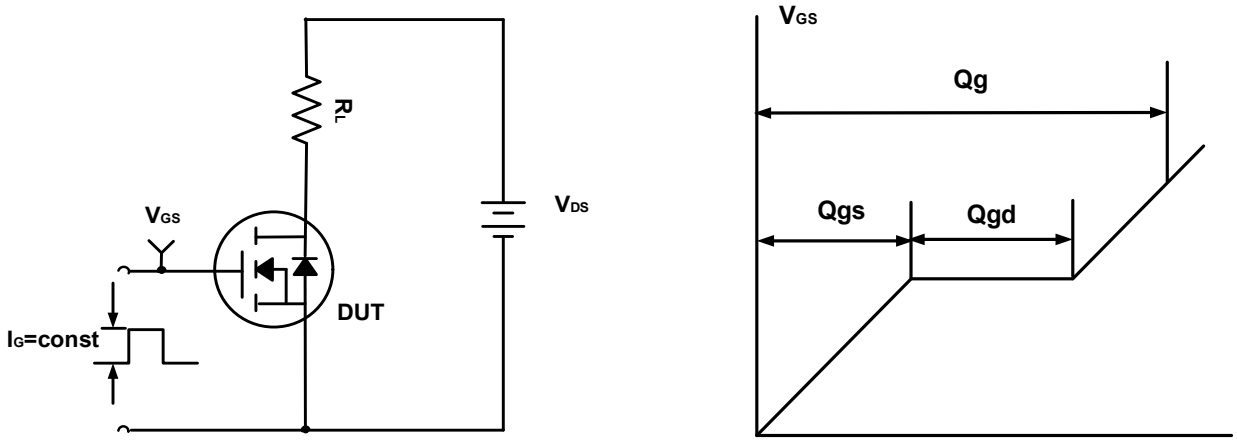


Figure A. Gate Charge Test Circuit & Waveforms

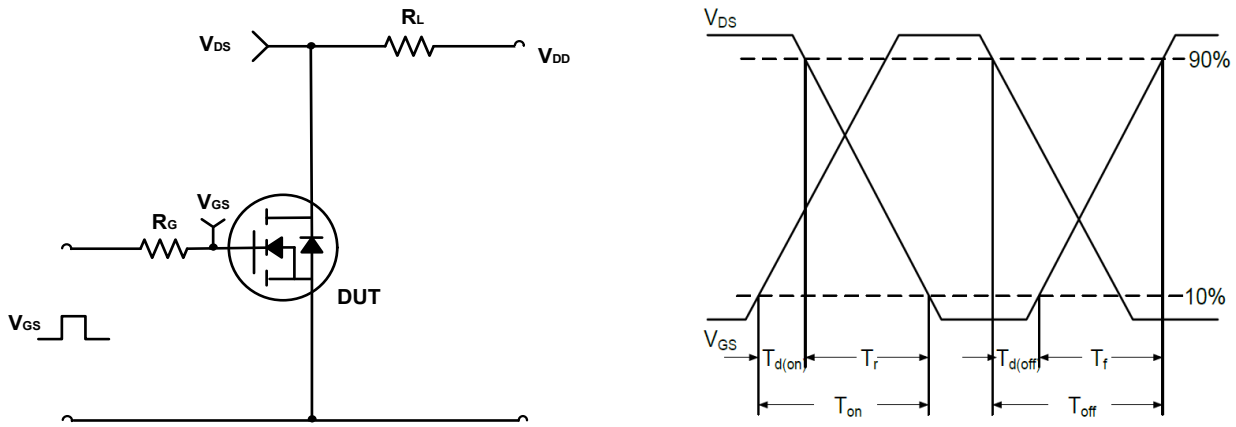


Figure B. Switching Test Circuit & Waveforms

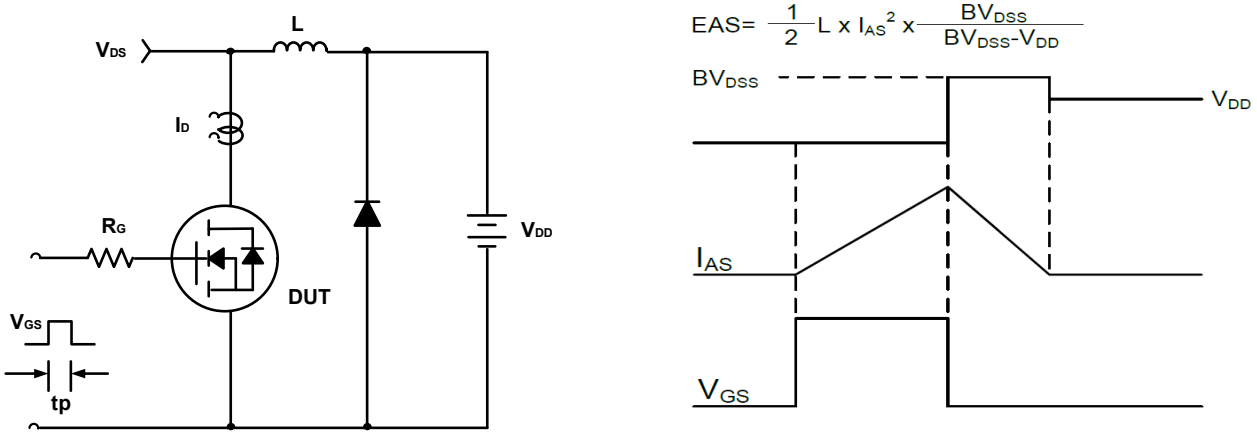
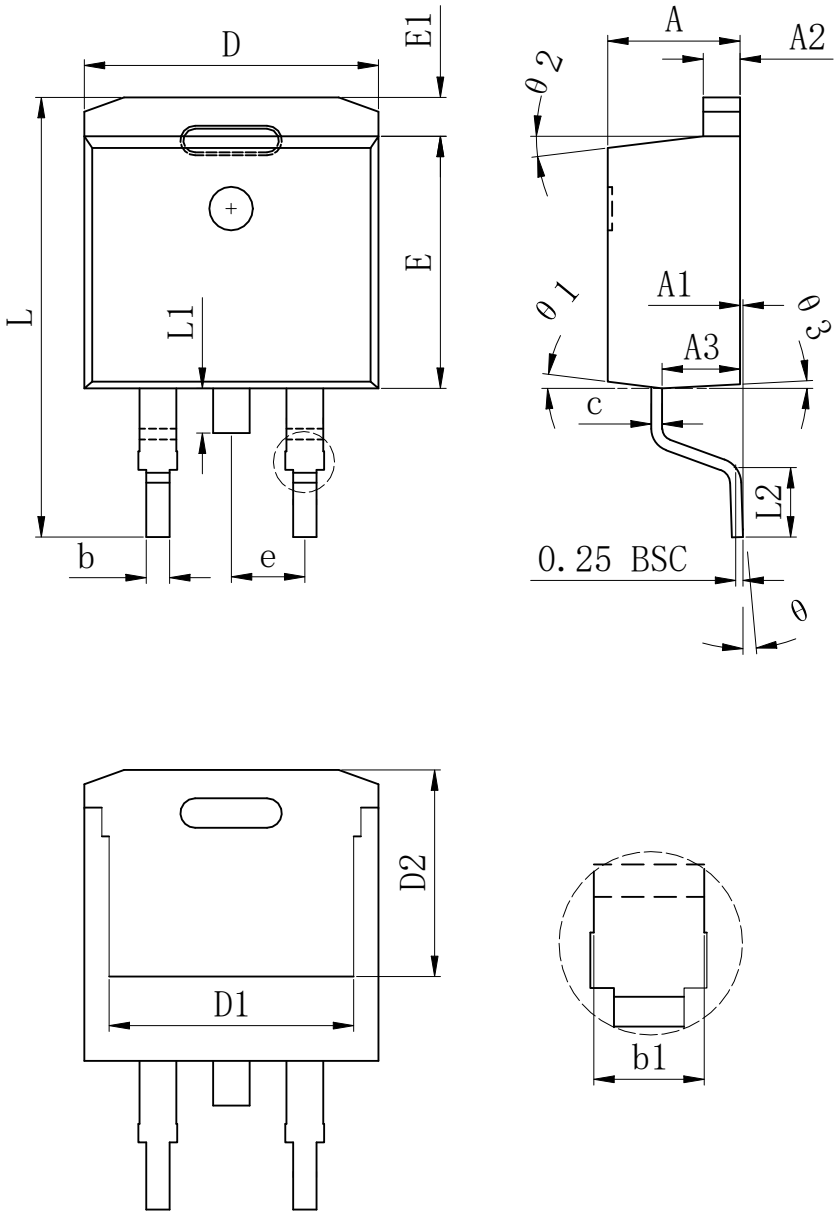


Figure C. Unclamped Inductive Switching Circuit & Waveforms

Mechanical Dimensions for TO-2LL



SYMBOL	MILLIMETER		
	MIN	Typ.	MAX
A	4.370	4.570	4.770
A1	0.000		0.250
A2	1.220	1.270	1.420
A3	2.490	2.690	2.890
b	0.700	0.810	0.960
b1	1.170	1.270	1.470
c	0.300	0.380	0.530
D	9.860	10.160	10.360
D1	8.400 REF		
D2	7.073 REF		
E	8.500	8.700	8.900
E1	1.070	1.270	1.470
e	2.540 TYP		
L	14.700	15.100	15.500
L1	1.400	1.550	1.700
L2	2.000	2.300	2.600
θ	0°		9°
θ1	7° TYP		
θ2	7° TYP		
θ3	3° TYP		