

● General Description

The TF030N04NG combines advanced trench MOSFET technology with a low resistance package to provide extremely low  $R_{DS(ON)}$ . This device is ideal for load switch and battery protection applications.

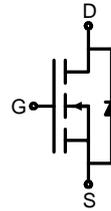
● Features

- Advance high cell density Trench technology
- Low  $R_{DS(ON)}$  to minimize conductive loss
- Low Gate Charge for fast switching
- Low Thermal resistance

● Application

- MB/VGA Vcore
- SMPS 2<sup>nd</sup> Synchronous Rectifier
- POL application
- BLDC Motor driver

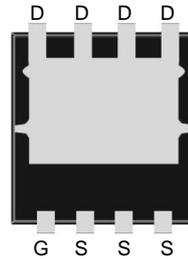
● Product Summary



$V_{DS} = 40V$   $I_D = 110A$

$R_{DS(ON)(10V\ typ)} = 2.5m\Omega$

$R_{DS(ON)(4.5V\ typ)} = 3.2m\Omega$



PDFNWB5x6-8L

● Ordering Information:

Part NO.	TF030N04NG
Marking 1	030N04NG: TF030N04NG
Marking 2	TF:tuofeng; AA:device code; Y:year code; X:Week
MOQ	5000

● Absolute Maximum Ratings ( $T_C = 25^\circ C$ )

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	$V_{DS}$	40	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current	$I_D @ T_C = 25^\circ C$	110	A
	$I_D @ T_C = 75^\circ C$	77	A
	$I_D @ T_C = 100^\circ C$	66	A
Pulsed Drain Current ①	$I_{DM}$	350	A
Total Power Dissipation	$P_D @ T_C = 25^\circ C$	70	W
Total Power Dissipation	$P_D @ T_A = 25^\circ C$	2.0	W
Operating Junction Temperature	$T_J$	-55 to 150	$^\circ C$
Storage Temperature	$T_{STG}$	-55 to 150	$^\circ C$

Note: ① Pulse Test : Pulse width  $\leq 300\mu s$ , Duty cycle  $\leq 2\%$  ;



Single Pulse Avalanche Energy	$E_{AS}$	120	mJ			
Avalanche Current	$I_{AS} I_{AR}$	25	A			
<b>●Thermal resistance</b>						
<b>Parameter</b>	<b>Symbol</b>	<b>Min.</b>	<b>Typ.</b>	<b>Max.</b>	<b>Unit</b>	
Thermal resistance, junction - case	$R_{thJC}$	-	-	3.0	° C/W	
Thermal resistance, junction - ambient	$R_{thJA}$	-	-	60	° C/W	
Soldering temperature, wave soldering for 8s	$T_{sold}$	-	-	265	° C	
<b>●Electronic Characteristics</b>						
<b>Parameter</b>	<b>Symbol</b>	<b>Condition</b>	<b>Min.</b>	<b>Typ</b>	<b>Max.</b>	<b>Unit</b>
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	40			V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	1.1	1.7	2.5	V
Drain-Source Leakage Current	$I_{DSS}$	$V_{DS} = 40V, V_{GS} = 0V$			1.0	$\mu A$
Gate- Source Leakage Current	$I_{GSS}$	$V_{GS} = \pm 20V, V_{DS} = 0V$			$\pm 100$	nA
Static Drain-source On Resistance	$R_{DS(ON)}$	$V_{GS} = 10V, I_D = 20A$		2.5	4.0	m $\Omega$
		$V_{GS} = 4.5V, I_D = 15A$		3.2	5.0	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS} = 10V, I_D = 20A$		60		S
Source-drain voltage	$V_{SD}$	$I_S = 20A$			1.20	V
<b>●Electronic Characteristics</b>						
<b>Parameter</b>	<b>Symbol</b>	<b>Condition</b>	<b>Min.</b>	<b>Typ</b>	<b>Max.</b>	<b>Unit</b>
Input capacitance	$C_{iss}$	$V_{ds} = 25V, V_{gs} = 0V$ $f = 1MHz$	-	1980	-	pF
Output capacitance	$C_{oss}$		-	455	-	
Reverse transfer capacitance	$C_{rss}$		-	29	-	
<b>●Gate Charge characteristics(<math>T_a = 25^\circ C</math>)</b>						
<b>Parameter</b>	<b>Symbol</b>	<b>Condition</b>	<b>Min.</b>	<b>Typ</b>	<b>Max.</b>	<b>Unit</b>
Gate Resistance	$R_g$	$f = 1MHz$		1.7		$\Omega$
Total gate charge	$Q_g$	$V_{DD} = 20V$ $I_D = 20A$ $V_{GS} = 10V$	-	32.0	-	nC
Gate - Source charge	$Q_{gs}$		-	4.70	-	
Gate - Drain charge	$Q_{gd}$		-	5.30	-	
Turn-ON Delay time	$t_{D(on)}$	$V_{GS} = 10V, V_{DS} = 20V$ $R_G = 3.0\Omega, I = 20A$		7.40		ns
Turn-ON Rise time	$t_r$			4.70		ns
Turn-Off Delay time	$t_{D(off)}$			29.2		ns
Turn-Off Fall time	$t_f$			7.30		ns

Typical Characteristics

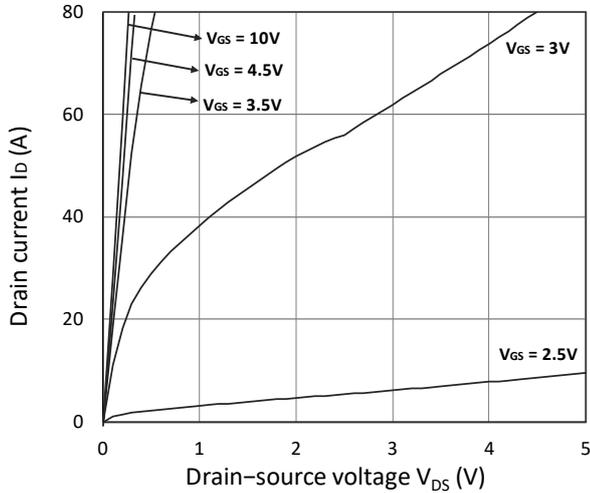


Figure 1. Output Characteristics

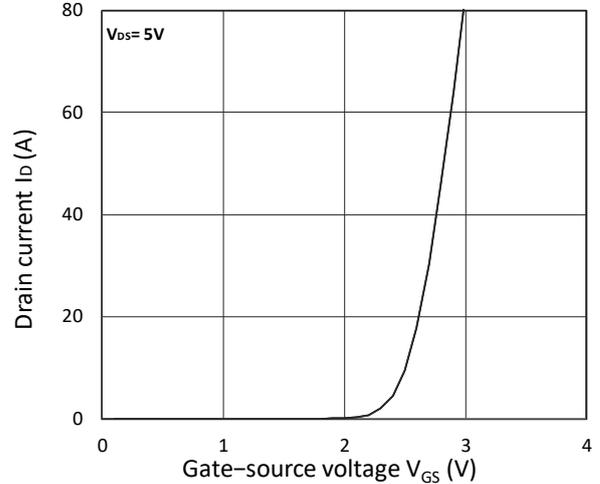


Figure 2. Transfer Characteristics

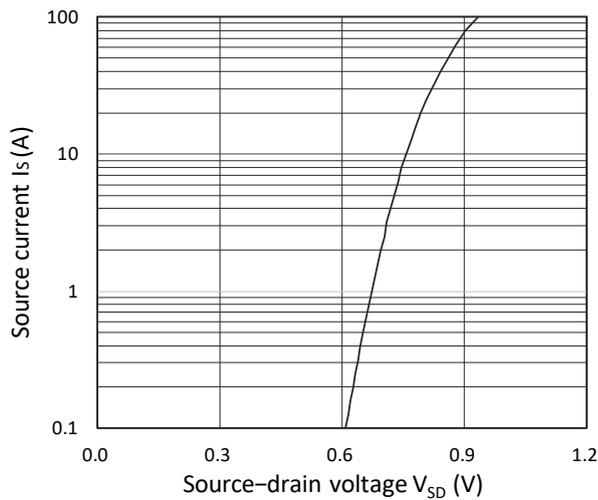


Figure 3. Forward Characteristics of Reverse

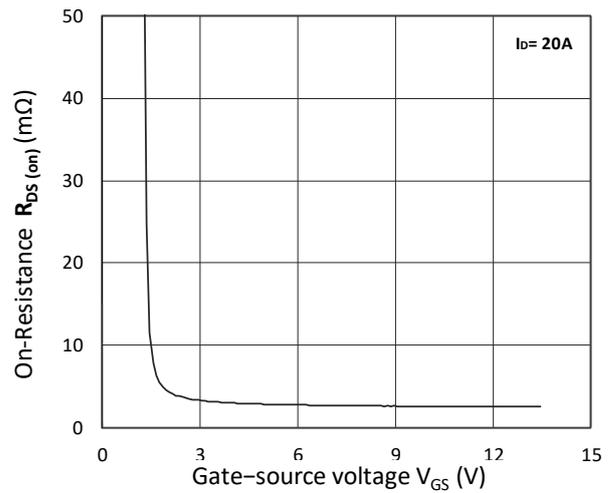


Figure 4.  $R_{DS(on)}$  vs.  $V_{GS}$

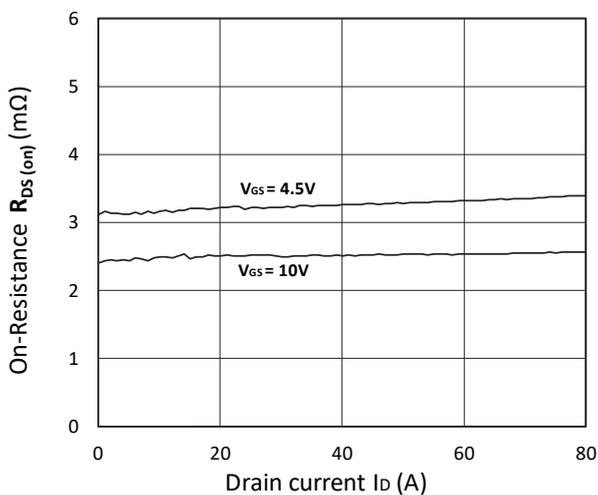


Figure 5.  $R_{DS(on)}$  vs.  $I_D$

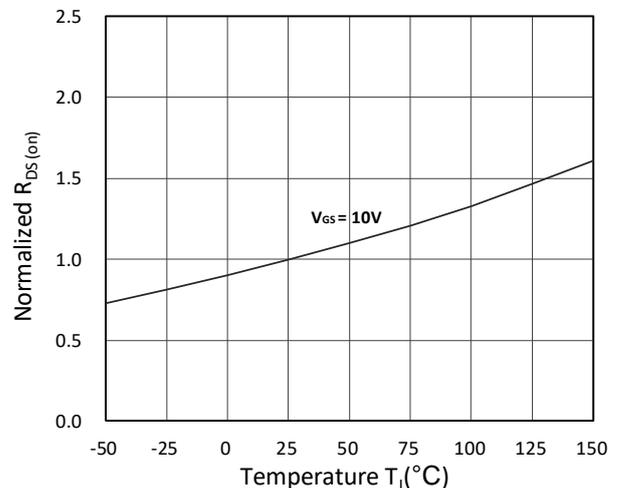


Figure 6. Normalized  $R_{DS(on)}$  vs. Temperature

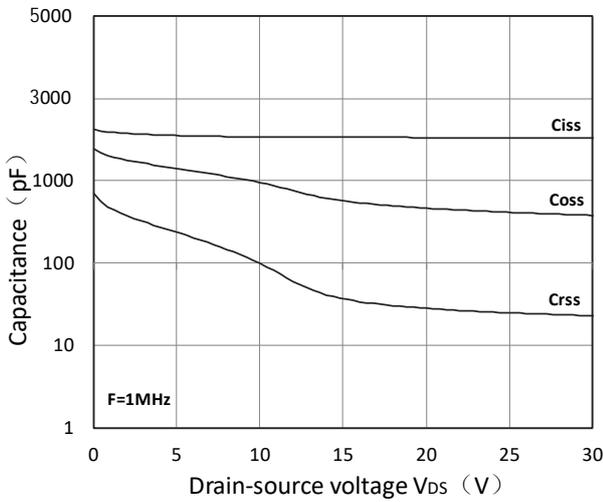


Figure 7. Capacitance Characteristics

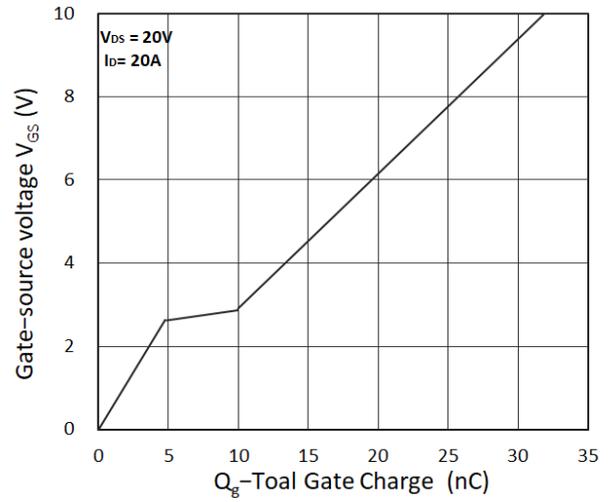


Figure 8. Gate Charge Characteristics

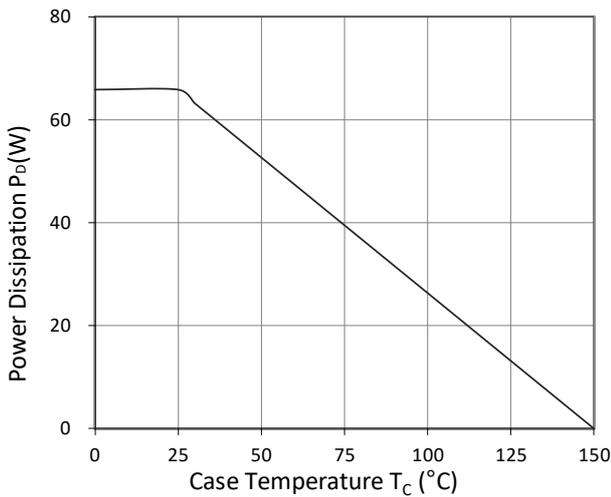


Figure 9. Power Dissipation

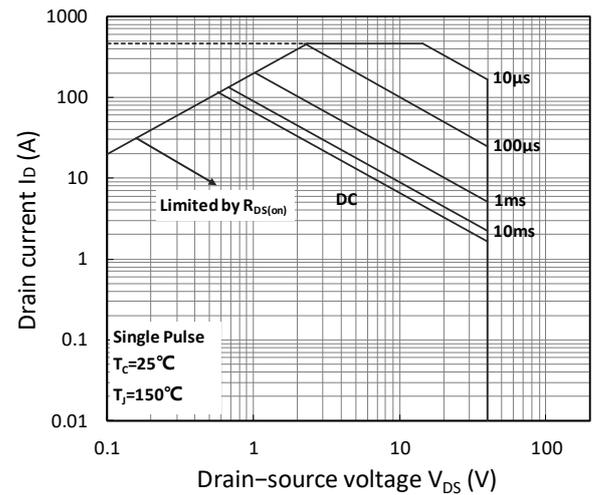


Figure 10. Safe Operating Area

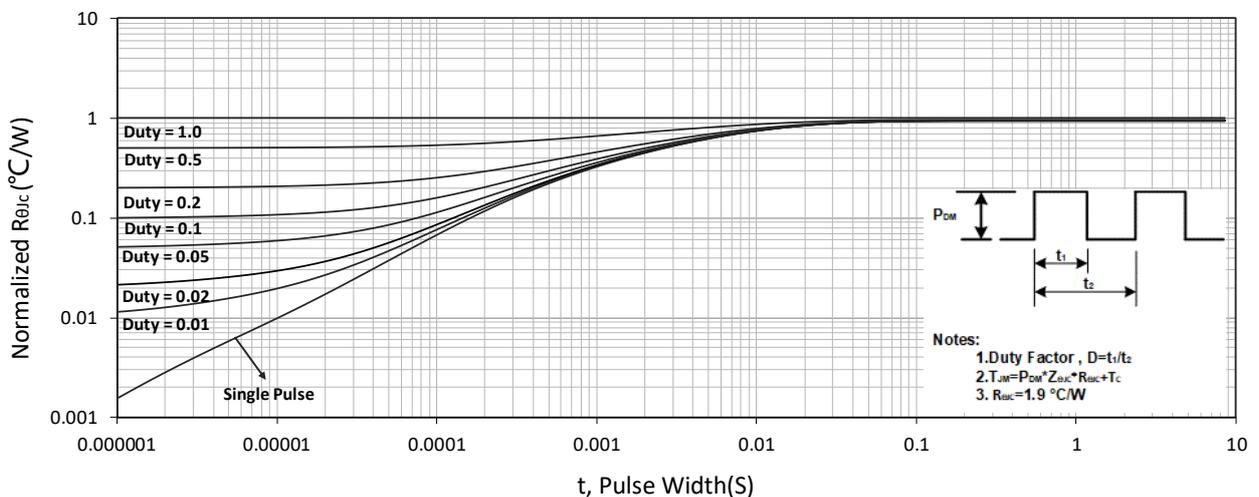
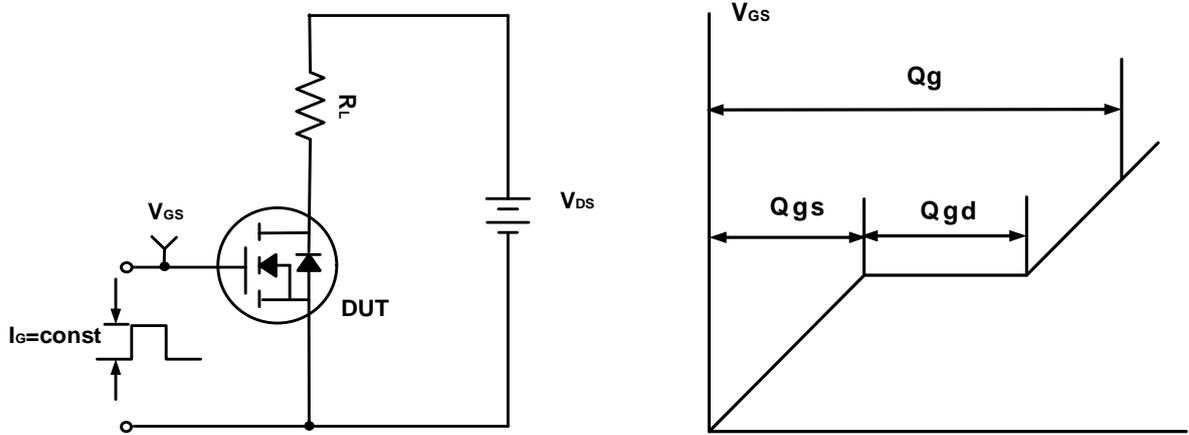
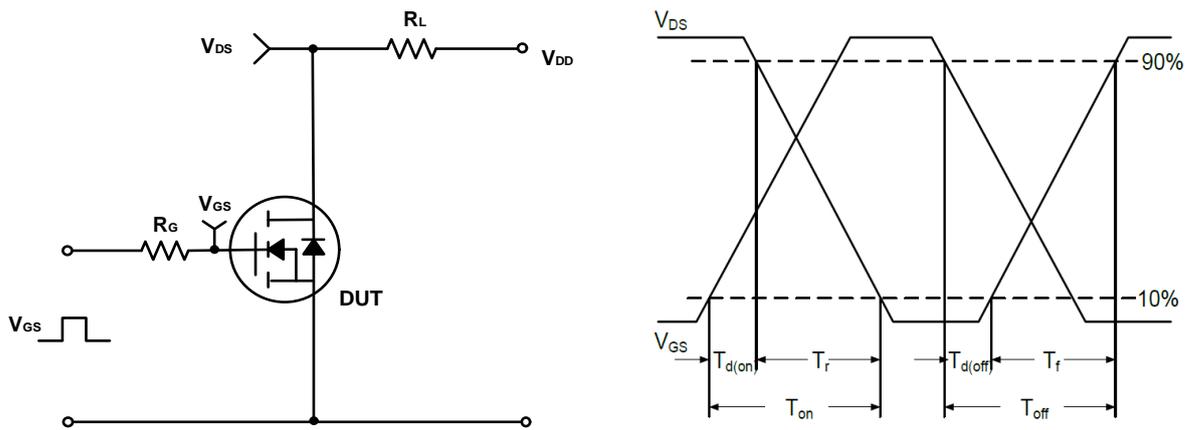


Figure 11. Normalized Maximum Transient Thermal Impedance

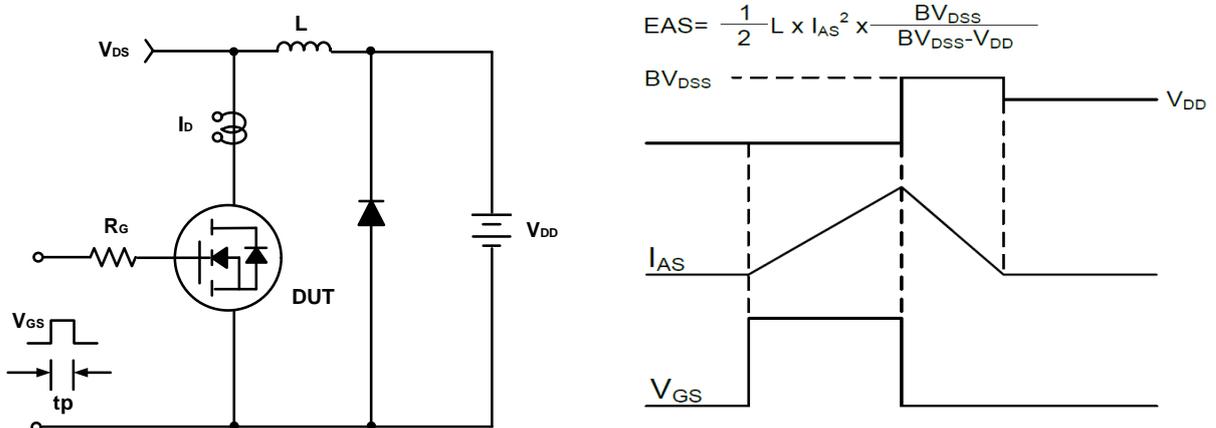
**Test Circuit**



**Figure A. Gate Charge Test Circuit & Waveforms**

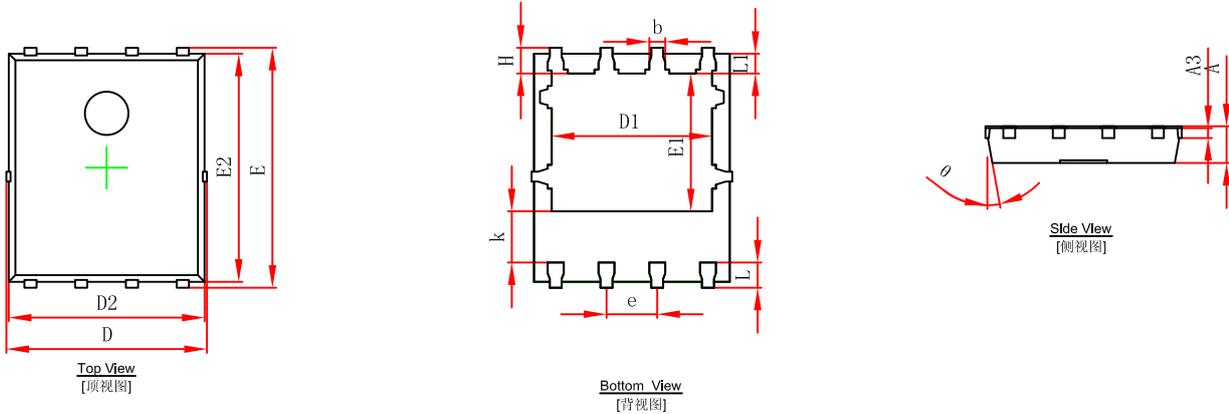


**Figure B. Switching Test Circuit & Waveforms**



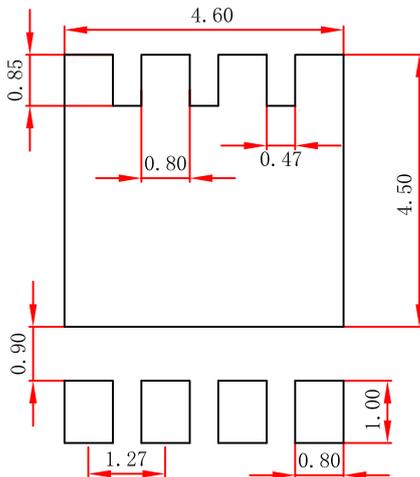
**Figure C. Unclamped Inductive Switching Circuit & Waveforms**

PDFNWB5x6-8L Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	10°	12°	10°	12°

PDFNWB5x6-8L Suggested Pad Layout



- Note:
1. Controlling dimension: in millimeters.
  2. General tolerance:  $\pm 0.05$ mm.
  3. The pad layout is for reference purposes only.