



Shenzhen Tuofeng Semiconductor Technology Co., Ltd

**N - CHANNEL ENHANCEMENT MODE POWER MOSFET****TF020N02N****• General Description**

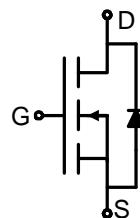
The TF020N02N combines advanced trench MOSFET technology with a low resistance package to provide extremely low  $R_{DS(ON)}$ .

**• Features**

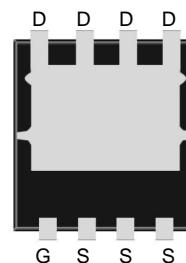
- Advance high cell density Trench technology
- Low  $R_{DS(ON)}$  to minimize conductive loss
- Low Gate Charge for fast switching
- Low Thermal resistance

**• Application**

- MB/VGA Vcore
- SMPS 2<sup>nd</sup> Synchronous Rectifier
- POL application
- BLDC Motor driver

**• Product Summary**

$V_{DS} = 20V$   $I_D = 130A$   
 $R_{DS(on)(10V\ typ)} = 1.6m\Omega$   
 $R_{DS(on)(4.5V\ typ)} = 1.8m\Omega$   
 $R_{DS(on)(2.5V\ typ)} = 2.5m\Omega$

**PDFNWB5x6-8L****• Ordering Information:**

Part NO.	TF020N02N
Marking1	020N02N:TF020N02N
Marking2	TF:tuofeng; Y:year code; X:Week; AA:device code;
Basic ordering unit (pcs)	5000

**• Absolute Maximum Ratings ( $T_j=25^\circ C$ , unless otherwise noted)**

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	$V_{DS}$	20	V
Gate-Source Voltage	$V_{GS}$	$\pm 12$	V
Continuous Drain Current	$I_D @ T_C=25^\circ C$	130	A
	$I_D @ T_C=75^\circ C$	91	A
	$I_D @ T_C=100^\circ C$	78	A
Pulsed Drain Current <sup>①</sup>	$I_{DM}$	450	A
Total Power Dissipation <sup>②</sup>	$P_D @ T_C=25^\circ C$	75	W
Total Power Dissipation	$P_D @ T_A=25^\circ C$	1.5	W
Operating Junction Temperature	$T_J$	-55 to 150	°C
Storage Temperature	$T_{STG}$	-55 to 150	°C



Shenzhen Tuofeng Semiconductor Technology Co., Ltd

**N - CHANNEL ENHANCEMENT MODE POWER MOSFET****TF020N02N****•Thermal resistance**

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance, junction - case <sup>②</sup>	R <sub>thJC</sub>	-	-	1.6	° C/W
Thermal resistance, junction - ambient	R <sub>thJA</sub>	-	-	45	° C/W
Soldering temperature, wavesoldering for 8s	T <sub>sold</sub>	-	-	265	° C

**•Electronic Characteristics(T<sub>j</sub>=25 °C, unless otherwise note)**

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	20			V
Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250μA	0.5	0.9	1.3	V
Drain-Source Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0V			1.0	μA
Gate- Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±12V, V <sub>DS</sub> = 0V			±100	nA
Static Drain-source On Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 20A		1.6	2.0	mΩ
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 20A		1.8	2.5	mΩ
		V <sub>GS</sub> = 2.5V, I <sub>D</sub> = 20A		2.5	3.8	mΩ
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = 10V, I <sub>D</sub> = 20A		18		S
Source-drain voltage	V <sub>SD</sub>	I <sub>S</sub> = 20A		0.80	1.00	V

**•Electronic Characteristics**

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Input capacitance	C <sub>iss</sub>	V <sub>DD</sub> = 10V f = 1MHz V <sub>GS</sub> = 0V	-	6215	-	pF
Output capacitance	C <sub>oss</sub>		-	824	-	
Reverse transfer capacitance	C <sub>rss</sub>		-	723	-	

**•Gate Charge characteristics(T<sub>j</sub>=25 °C, unless otherwise note)**

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Total gate charge	Q <sub>g</sub>	V <sub>DD</sub> = 10V I <sub>D</sub> = 50A V <sub>GS</sub> = 10V	-	270	-	nC
Gate - Source charge	Q <sub>gs</sub>		-	15.0	-	
Gate - Drain charge	Q <sub>gd</sub>		-	50.0	-	
Turn-ON Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 10V, I <sub>D</sub> = 50A, R <sub>GEN</sub> = 3	-	21.0	-	nS
Rise Time	t <sub>r</sub>		-	28.0	-	
Turn-OFF Delay Time	t <sub>d(off)</sub>		-	31.0	-	
Fall Time	t <sub>f</sub>		-	25.0	-	

Note:

- ① Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2% ;
- ② Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate;

Fig.1 Gate-Charge Characteristics

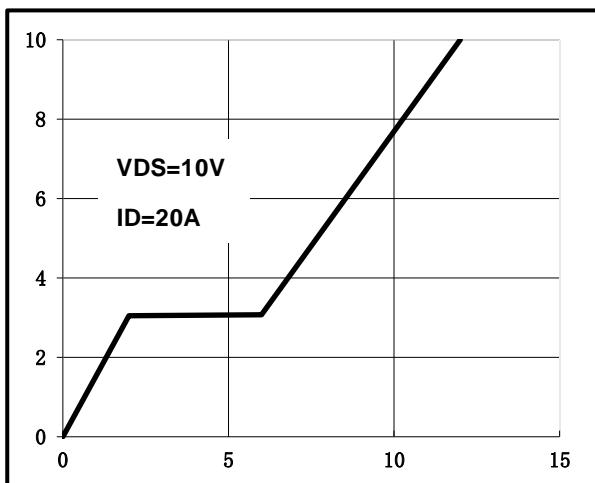


Fig.2 Capacitance Characteristics

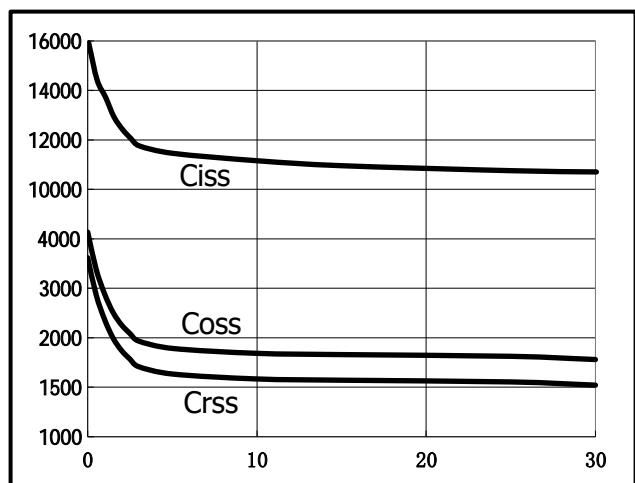


Fig.3 Power Dissipation Derating Curve

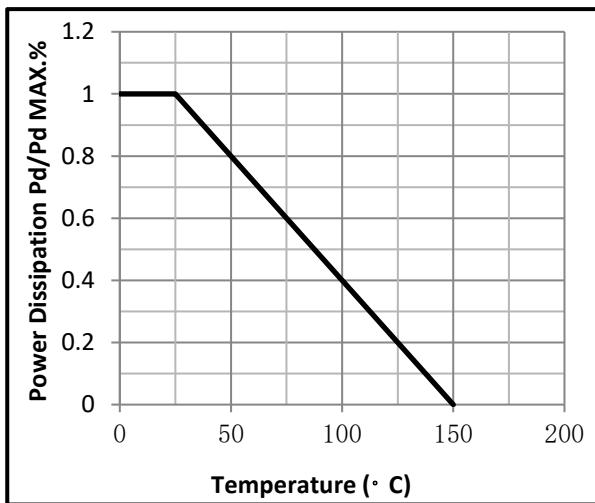


Fig.4 Typical output Characteristics

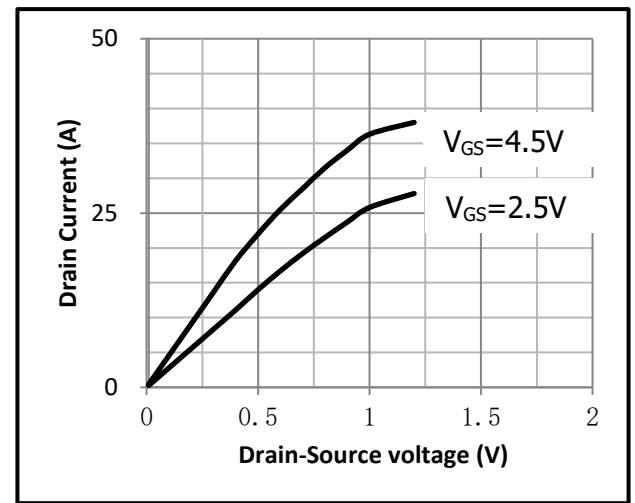


Fig.5 Threshold Voltage V.S Junction Temperature

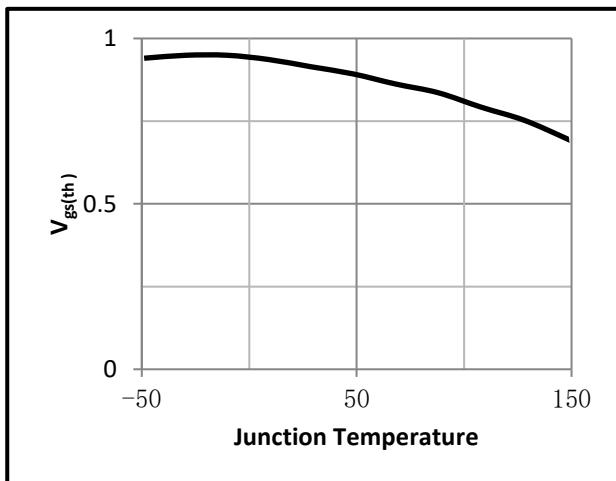


Fig.6 Resistance V.S Drain Current

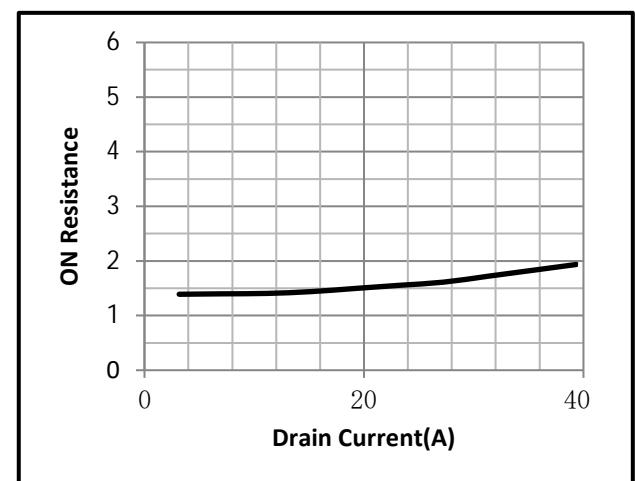


Fig.7 On-Resistance VS Gate Source Voltage

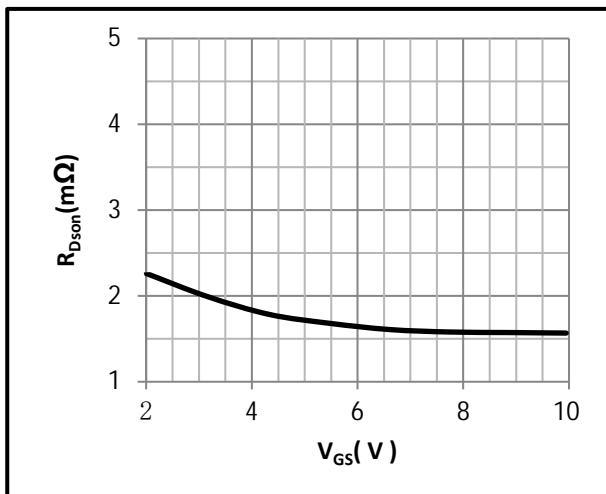


Fig.8 On-Resistance V.S Junction Temperature

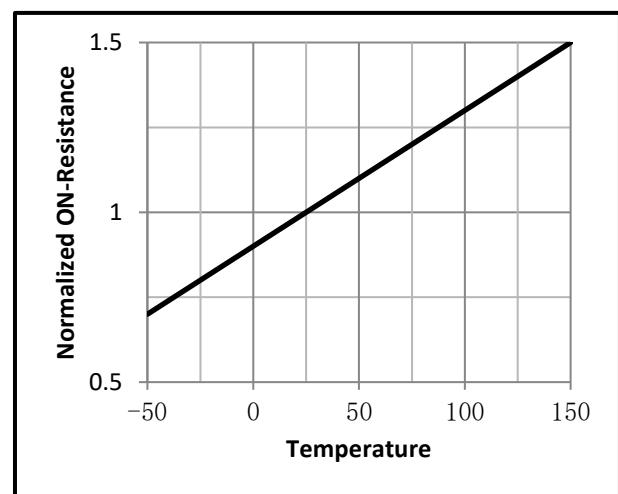


Fig.9 Switching Time Measurement Circuit

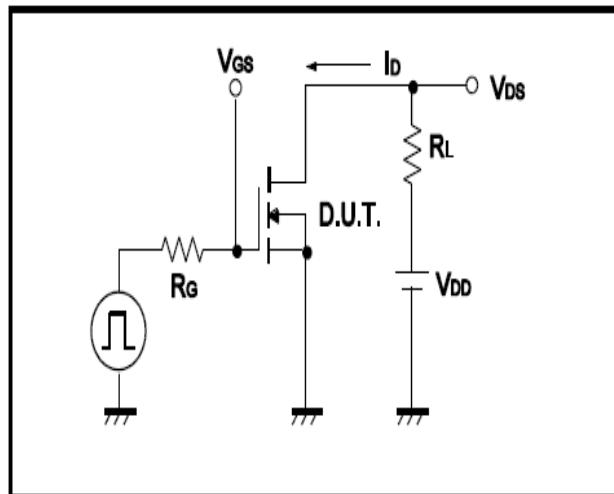


Fig.10 Gate Charge Waveform

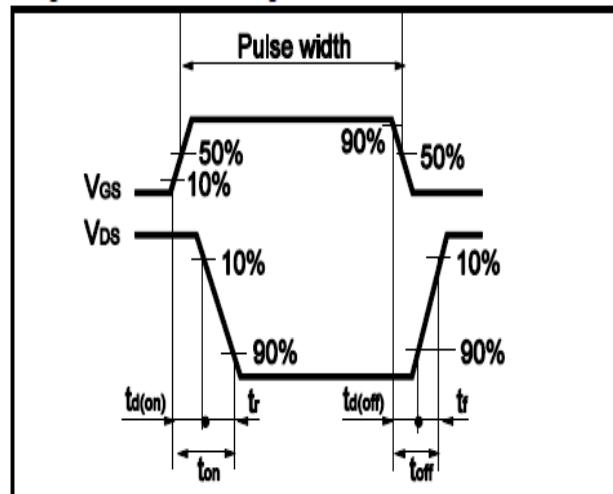


Fig.11 Avalanche Measurement Circuit

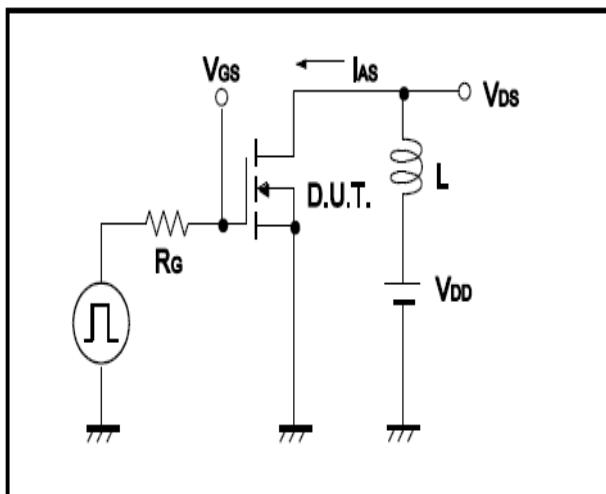
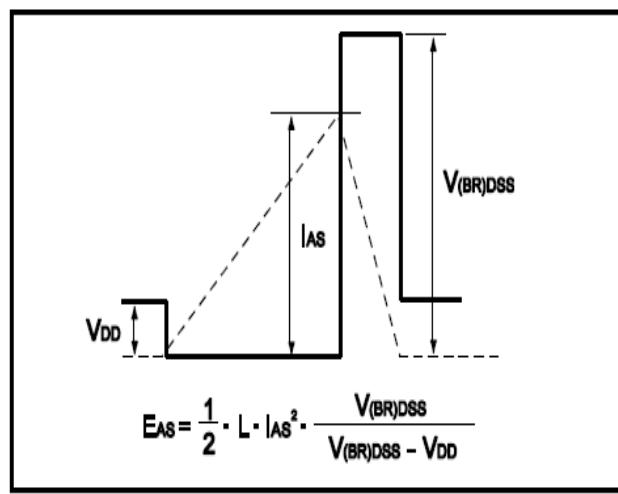
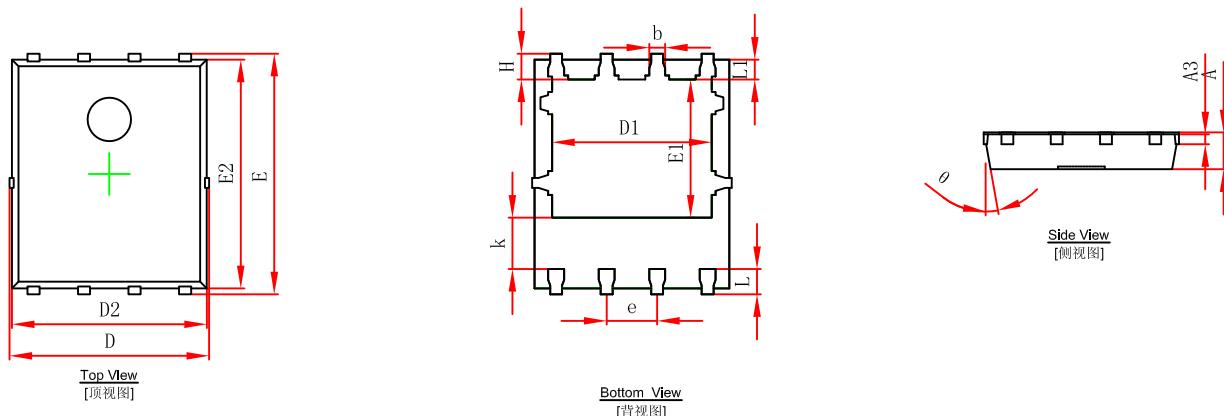


Fig.12 Avalanche Waveform

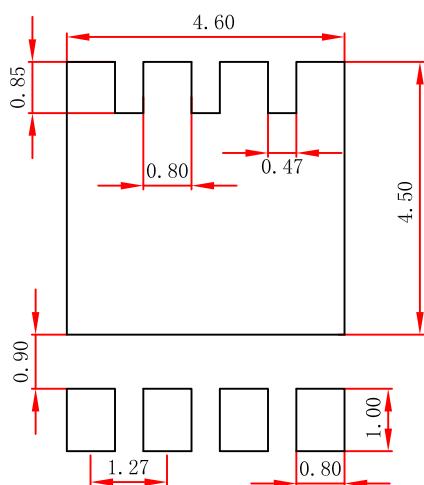




Shenzhen Tuofeng Semiconductor Technology Co., Ltd

**N - CHANNEL ENHANCEMENT MODE POWER MOSFET****TF020N02N****PDFNWB5x6-8L Package Outline Dimensions**

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	10°	12°	10°	12°

**PDFNWB5x6-8L Suggested Pad Layout****Note:**

1. Controlling dimension:in millimeters.
2. General tolerance: $\pm 0.05\text{mm}$ .
3. The pad layout is for reference purposes only.