

P-Channel Enhancement Mode Power MOSFET

Description

The TF4099 uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge . The complementary MOSFETs may be used to form a level shifted high side switch, and for a host of other applications.

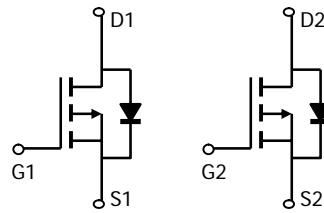
General Features

$V_{DS} = -40V$, $I_D = -7.0A$

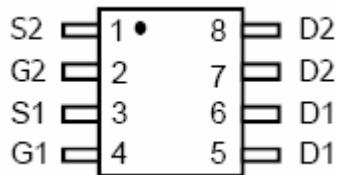
$R_{DS(ON)typ}$ $32m\Omega$ @ $V_{GS} = -10V$

$R_{DS(ON)typ}$ $43m\Omega$ @ $V_{GS} = -4.5V$

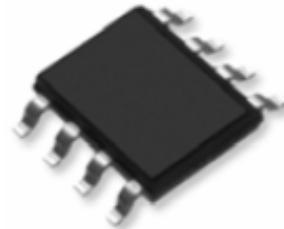
- High power and current handing capability
- Lead free product is acquired
- Surface mount package



Schematic diagram



Marking and pin assignment



SOP-8 top view

Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	-40	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^A	I_D	-7.0	A
Pulsed Drain Current ^B	I_{DM}	-25	
Power Dissipation ^A	P_D	2.0	W
		1.0	
Junction and Storage Temperature Range	T_J , T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	R_{0JA}	51	68	°C/W
Maximum Junction-to-Ambient ^A		61	115	°C/W
Maximum Junction-to-Lead ^C	R_{0JL}	45	55	°C/W



SHENZHEN TUOFENG SEMICONDUCTOR TECHNOLOGY CO., LTD

SOP-8 Plastic-Encapsulate MOSFETS

TF4099

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=-250\mu\text{A}, V_{GS}=0\text{V}$	-40			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-40\text{V}, V_{GS}=0\text{V}$			-100	nA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}, V_{GS}=\pm 20\text{V}$			± 100	nA
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu\text{A}$	-1.1	-1.7	-2.5	V
$I_{\text{D(ON)}}$	On state drain current	$V_{GS}=-4.5\text{V}, V_{DS}=-5\text{V}$	-20			A
$R_{\text{DS(ON)}}$	Static Drain-Source On-Resistance	$V_{GS}=-10\text{V}, I_D=-7.0\text{A}$		32	39	$\text{m}\Omega$
		$V_{GS}=-4.5\text{V}, I_D=-5.5\text{A}$		43	55	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS}=-5\text{V}, I_D=-7\text{A}$	15			S
V_{SD}	Diode Forward Voltage	$I_S=-7\text{A}, V_{GS}=0\text{V}$		-0.82	-1	V
I_S	Maximum Body-Diode Continuous Current				-7.0	A

DYNAMIC PARAMETERS

C_{iss}	Input Capacitance	$V_{GS}=0\text{V}, V_{DS}=-20\text{V}, f=1\text{MHz}$		1021		pF
C_{oss}	Output Capacitance			63.6		pF
C_{rss}	Reverse Transfer Capacitance			48.6		pF
R_g	Gate resistance	$V_{GS}=0\text{V}, V_{DS}=0\text{V}, f=1\text{MHz}$		4.7		Ω

SWITCHING PARAMETERS

$Q_g(10\text{V})$	Total Gate Charge (10V)	$V_{GS}=-10\text{V}, V_{DS}=-20\text{V}, I_D=-7\text{A}$		26.5		nC
$Q_g(4.5\text{V})$	Total Gate Charge (4.5V)			19.3		nC
Q_{gs}	Gate Source Charge			2.5		nC
Q_{gd}	Gate Drain Charge			5.5		nC
$t_{\text{D(on)}}$	Turn-On Delay Time	$V_{GS}=-10\text{V}, V_{DS}=-20\text{V}, I_D=-7\text{A}, R_{\text{GEN}}=10\Omega$		13.0		ns
t_r	Turn-On Rise Time			16.0		ns
$t_{\text{D(off)}}$	Turn-Off Delay Time			180		ns
t_f	Turn-Off Fall Time			86.0		ns
t_{rr}	Body Diode Reverse Recovery Time		$I_F=-7\text{A}, dI/dt=100\text{A}/\mu\text{s}$	34.0		ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=-7\text{A}, dI/dt=100\text{A}/\mu\text{s}$		35.0		nC

A: The value of R_{0JA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The value in any given application depends on the user's specific board design. The current rating is based on the $t \leq 10\text{s}$ thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C. The R_{0JA} is the sum of the thermal impedance from junction to lead R_{0JL} and lead to ambient.

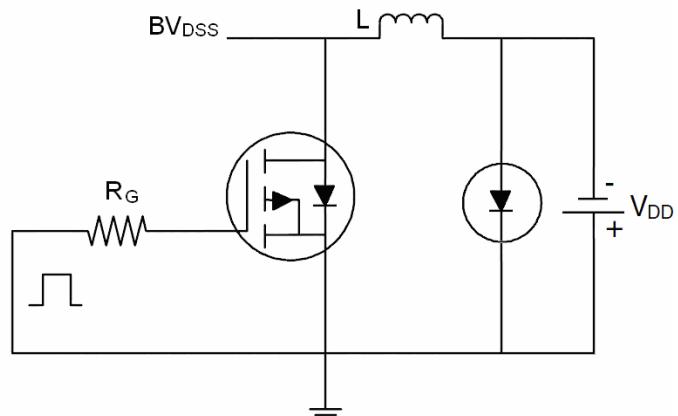
D. The static characteristics in Figures 1 to 6,12,14 are obtained using 80 μs pulses, duty cycle 0.5% max.

E. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The SOA curve provides a single pulse rating.

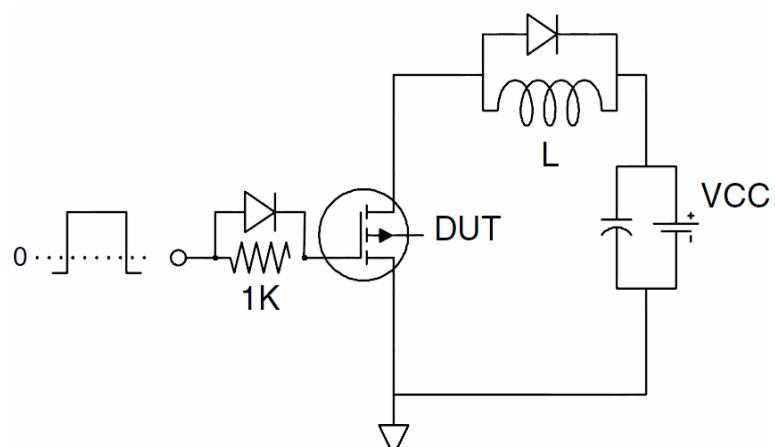
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Test Circuit

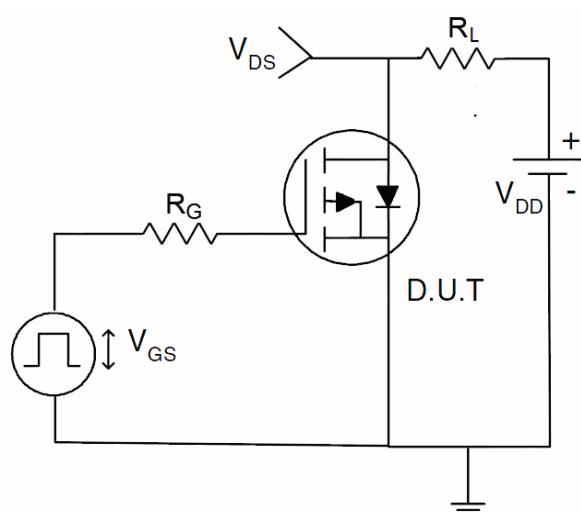
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit



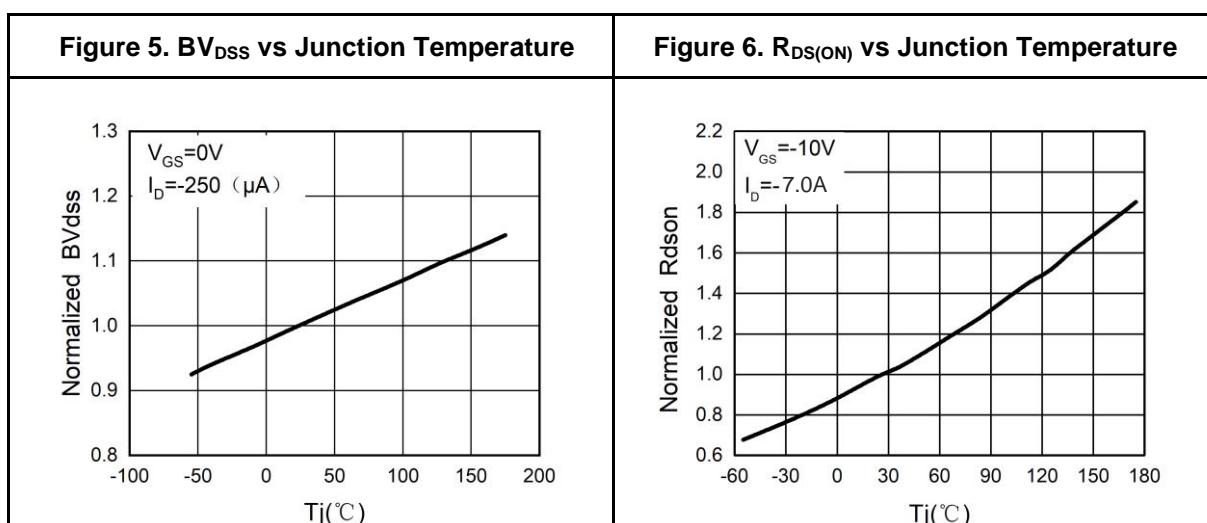
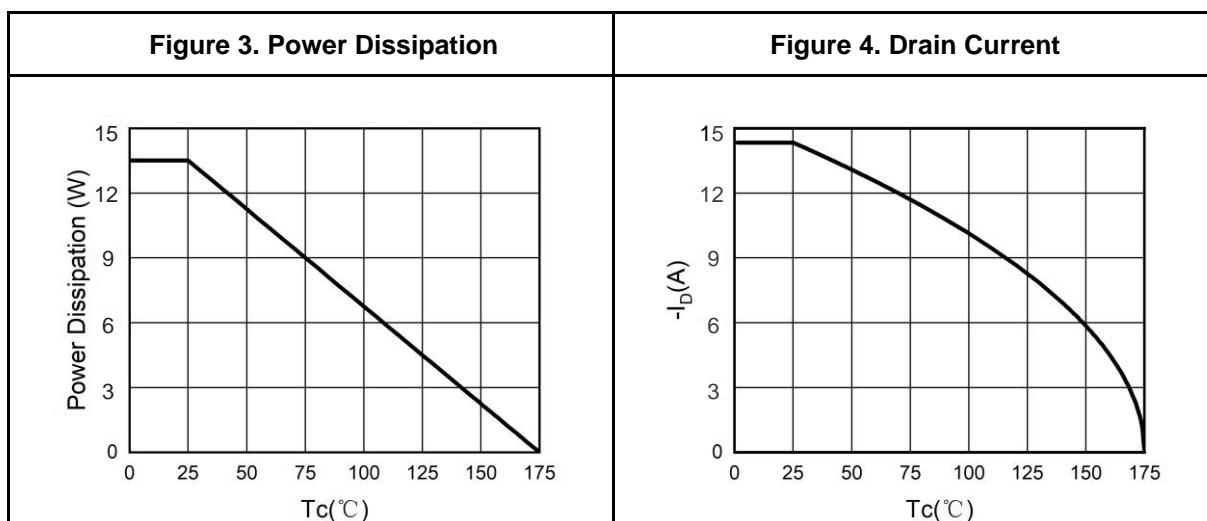
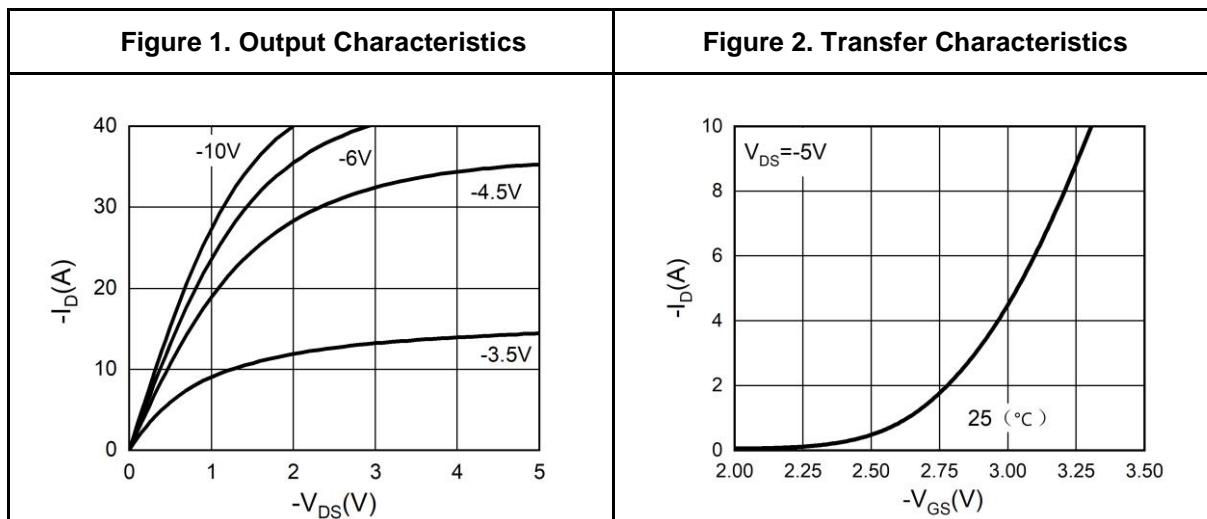
3) Switch Time Test Circuit



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Typical Electrical And Thermal Characteristics (Curves)



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Figure 7. Gate Charge Waveforms

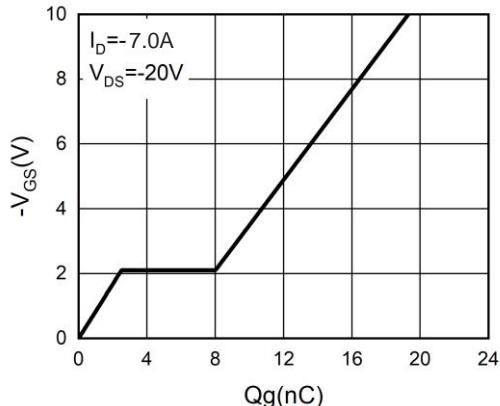


Figure 8. Capacitance

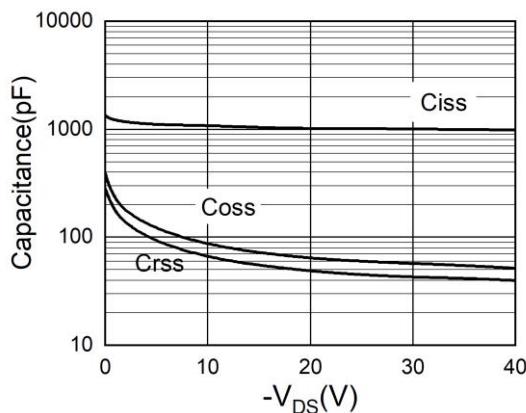


Figure 9. Body-Diode Characteristics

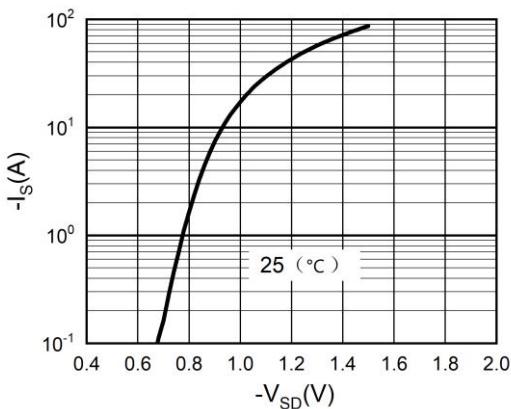
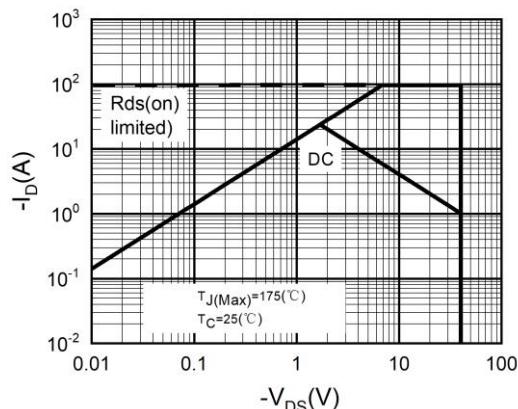
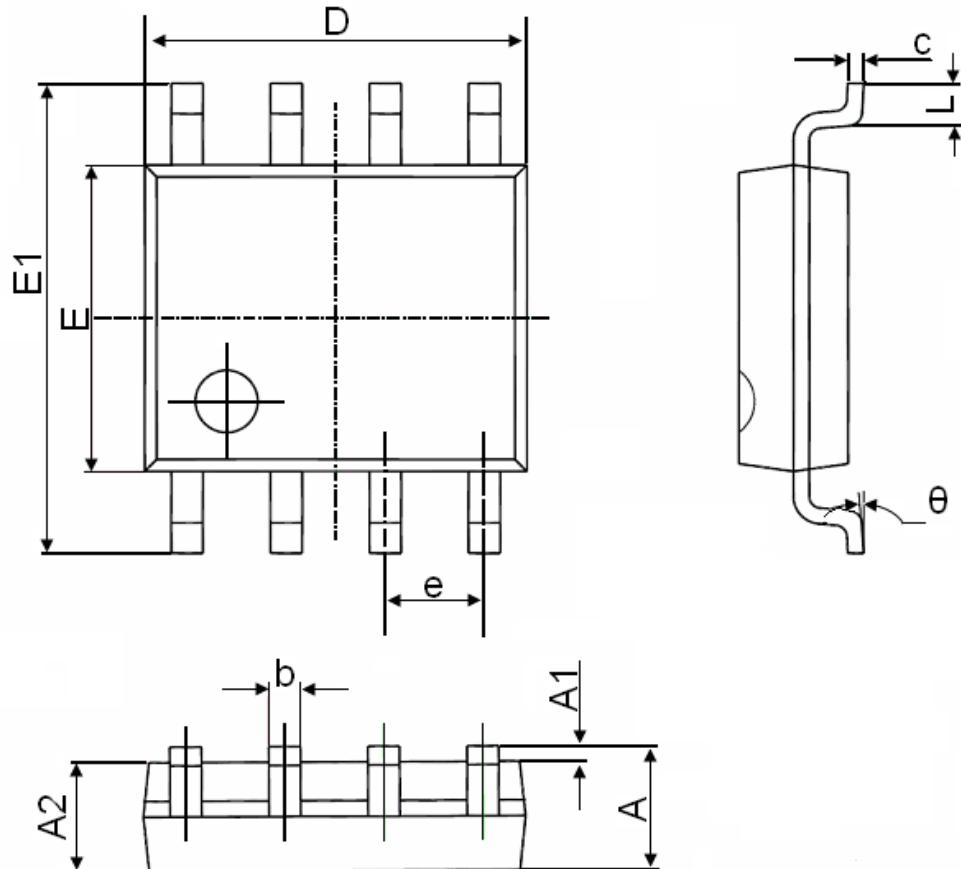


Figure 10. Maximum Safe Operating Area



SOP-8 Package Information


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°