

General Description

The TF060P03M combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$.

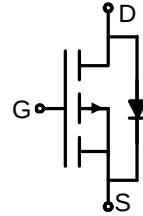
Features

Advance high cell density Trench technology
Low $R_{DS(ON)}$ to minimize conductive loss
Low Gate Charge for fast switching
Low Thermal resistance

Application

MB/VGA Vcore
SMPS 2nd Synchronous Rectifier
POL application
BLDC Motor driver

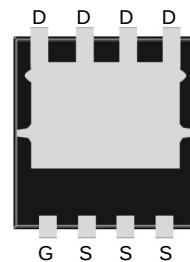
Product Summary



$$V_{DS} = -30V \quad I_D = -70A$$

$$R_{DS(ON)}(-10V \text{ typ}) = 5.7m\Omega$$

$$R_{DS(ON)}(-4.5V \text{ typ}) = 7.8m\Omega$$



PDFNWB3.3x3.3-8L

Ordering Information:

Part NO.	TF060P03M
Marking1	TF060P03M
Marking2	TF:tuofeng; Y:year code; X:Week; AA:device code;
Basic ordering unit (pcs)	5000

Absolute Maximum Ratings ($T_C = 25^\circ C$)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	$I_{D@T_C=25^\circ C}$	-70	A
	$I_{D@T_C=75^\circ C}$	-49	A
	$I_{D@T_C=100^\circ C}$	-42	A
Pulsed Drain Current ^①	I_{DM}	-190	A
Total Power Dissipation ^②	$P_D@T_C=25^\circ C$	65	W
Total Power Dissipation	$P_D@T_A=25^\circ C$	2.0	W
Operating Junction Temperature	T_J	-55 to 150	$^\circ C$
Storage Temperature	T_{STG}	-55 to 150	$^\circ C$

●Thermal resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance, junction - case ^②	R _{thJC}	-	-	4.2	° C/W
Thermal resistance, junction - ambient	R _{thJA}	-	-	55	° C/W
Soldering temperature, wavesoldering for 8s	T _{sold}	-	-	265	° C

●Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D = -250uA	-30			V
Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = -250uA	-1.0	-1.6	-2.0	V
Drain-Source Leakage Current	I _{DSS}	V _{DS} = -28V, V _{GS} = 0V			-1.0	uA
Gate- Source Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} = 0V			±100	nA
Static Drain-source On Resistance	R _{DS(ON)}	V _{GS} = -10V, I _D = -20A		5.7	7.0	mΩ
		V _{GS} = -4.5V, I _D = -10A		7.8	9.5	mΩ
Forward Transconductance	g _{FS}	V _{DS} = -10V, I _D = -10A		12		S
Source-drain voltage	V _{SD}	I _S = -20A		0.85	1.00	V

●Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Input capacitance	C _{iss}	f = 1MHz V _{DD} = -15V V _{GS} = 0V	-	3151	-	pF
Output capacitance	C _{oss}		-	359	-	
Reverse transfer capacitance	C _{rss}		-	343	-	

●Gate Charge characteristics(T_a = 25°C)

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Total gate charge	Q _g	V _{DD} = -15V I _D = -20A V _{GS} = -10V	-	85.0	-	nC
Gate - Source charge	Q _{gs}		-	14.0	-	
Gate - Drain charge	Q _{gd}		-	16.0	-	
Turn-On Delay Time	t _{d(on)}	V _{DD} = -15V V _{GS} = -10V R _L = 3Ω I _D = -20A	-	11.0	-	ns
Turn-On Rise Time	t _r		-	48.0	-	ns
Turn-Off Delay Time	t _{d(off)}		-	76.0	-	ns
Turn-Off Fall Time	t _f		-	45.0	-	ns

Note:

① Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2% ;

Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate;

P- Channel Typical Characteristics (Continued)

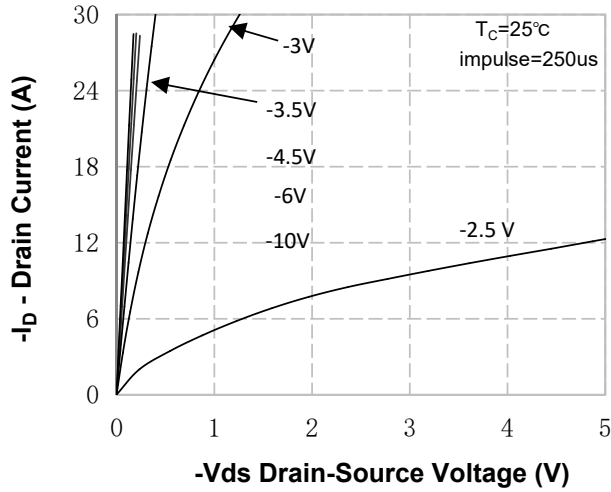


Figure 1. On-Region Characteristics

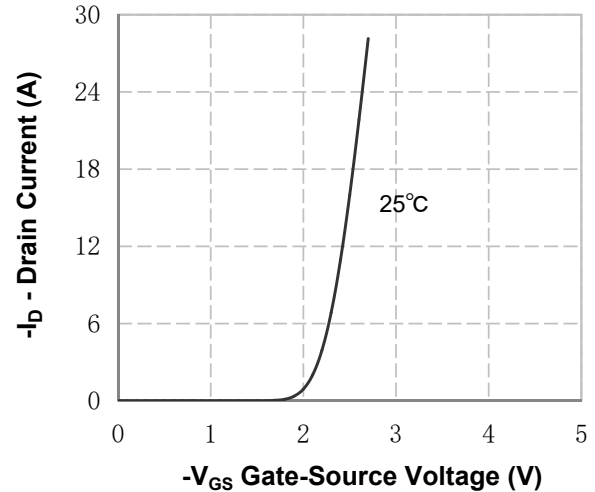


Figure 2. Transfer Characteristics

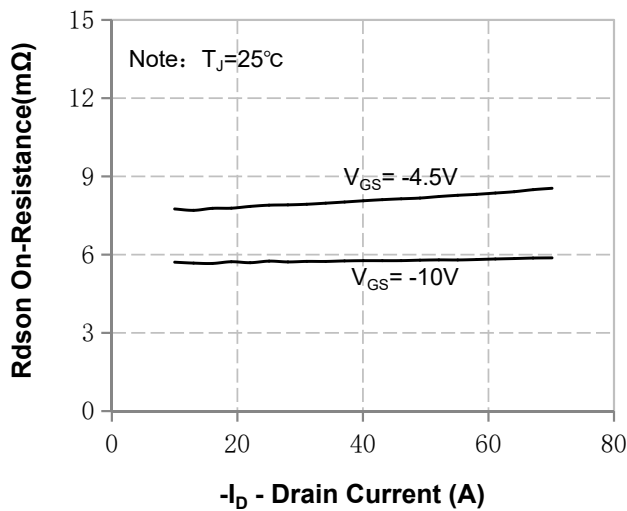


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

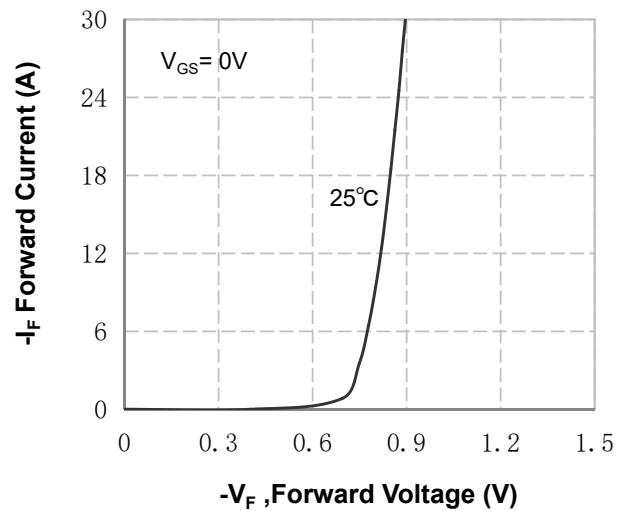


Figure 4. Body Diode Forward Voltage Variation with Source Current

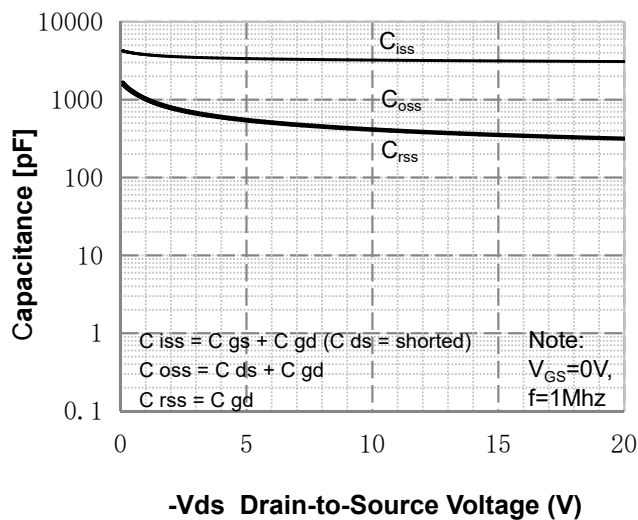


Figure 5. Capacitance Characteristics

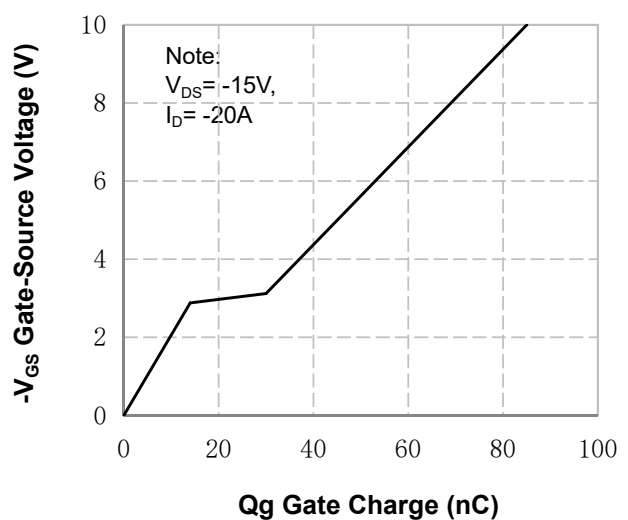


Figure 6. Gate Charge Characteristics

P- Channel Typical Characteristics (Continued)

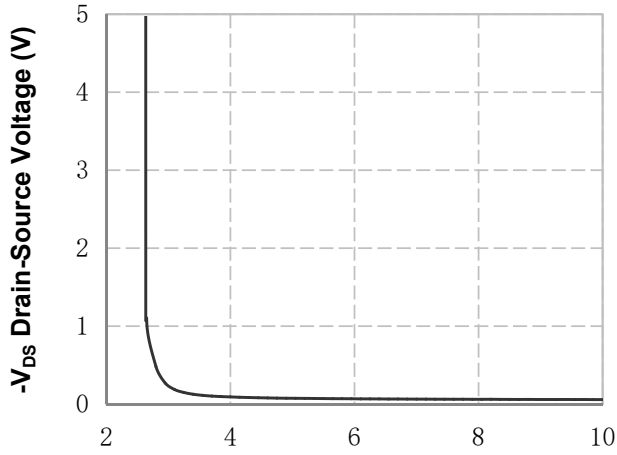


Figure 7. V_{ds} Drain-Source Voltage vs Gate Voltage

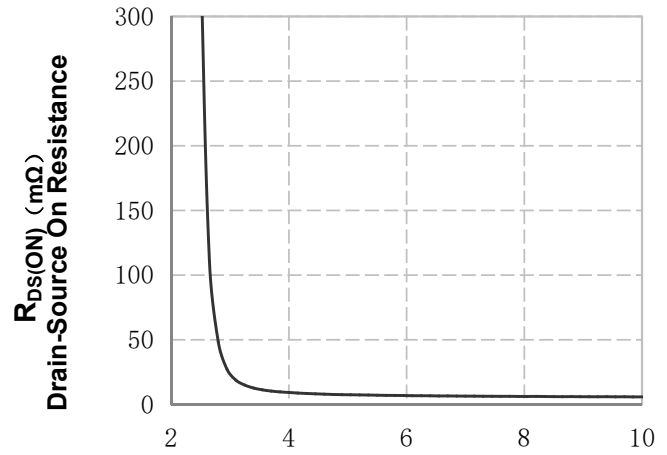


Figure 8. On-Resistance vs Gate Voltage

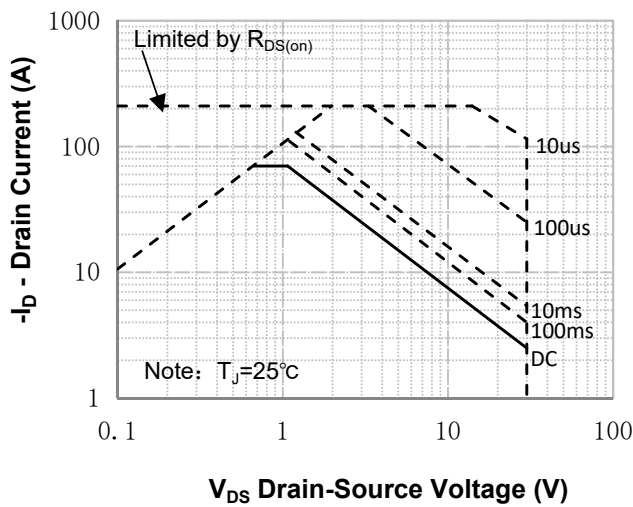


Figure 9. Maximum Safe Operating Area

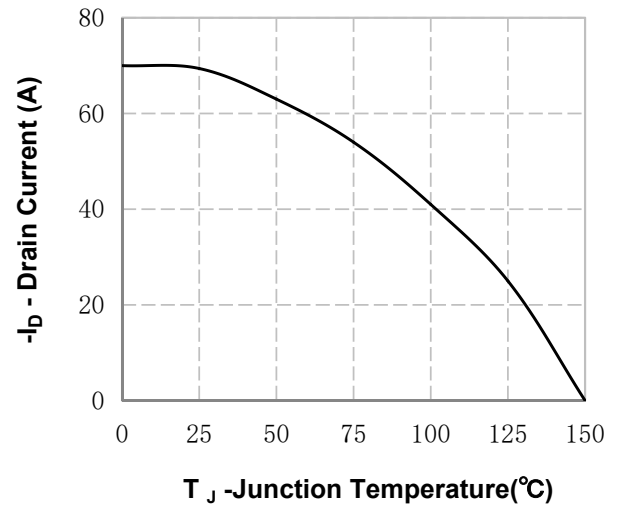


Figure 10. Maximum Continuous Drain Current vs Temperature

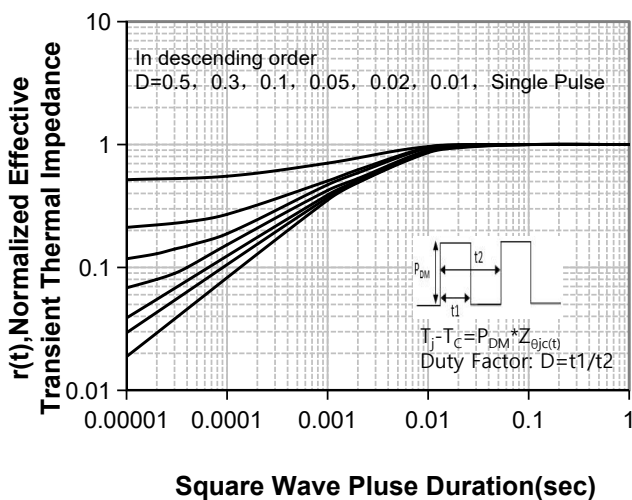
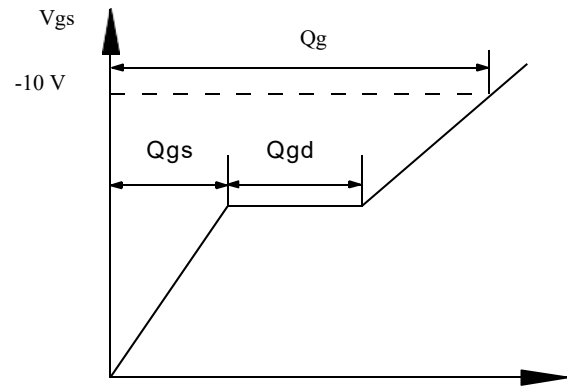
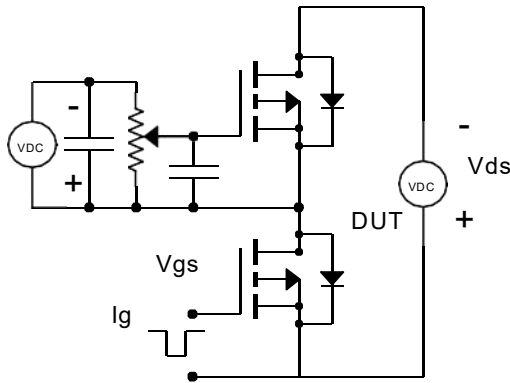
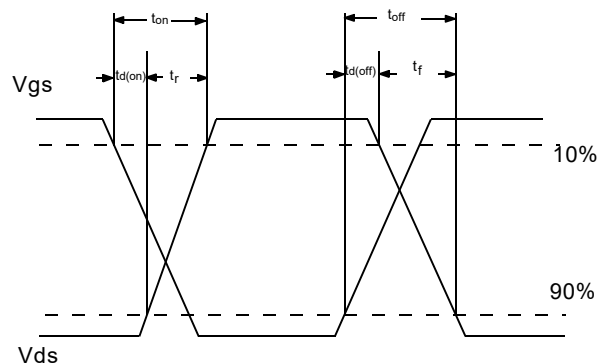
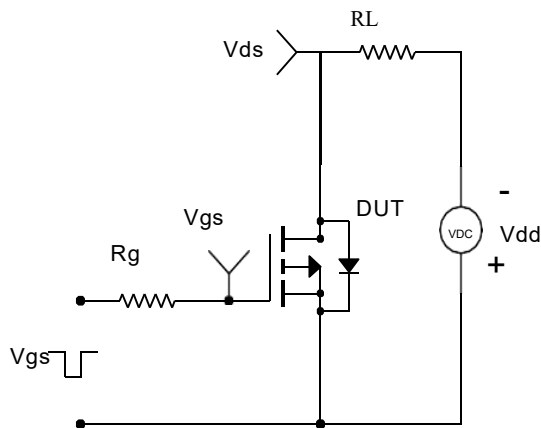


Figure 11. Transient Thermal Response Curve

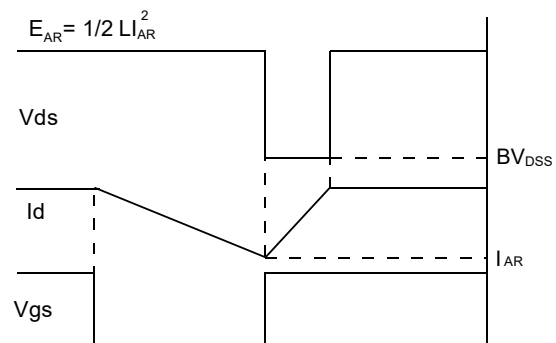
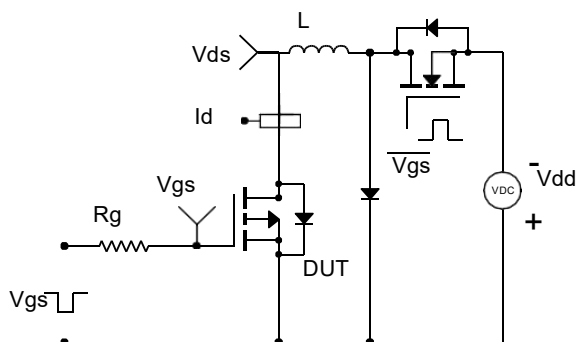
Gate Charge Test Circuit & Waveform



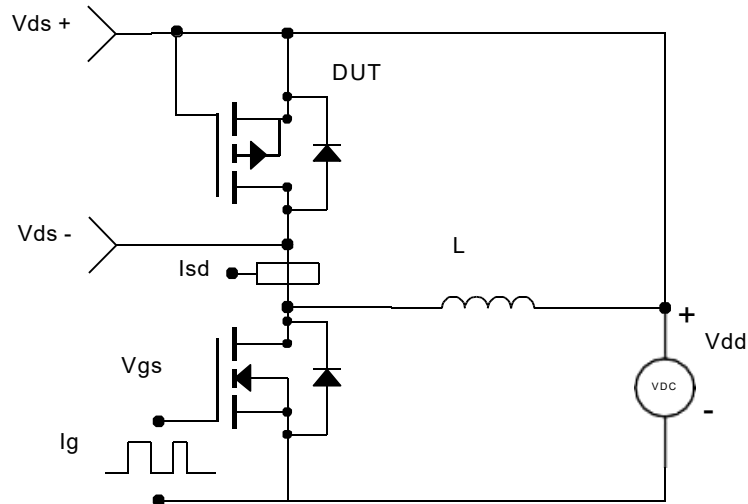
Resistive Switching Test Circuit & Waveforms



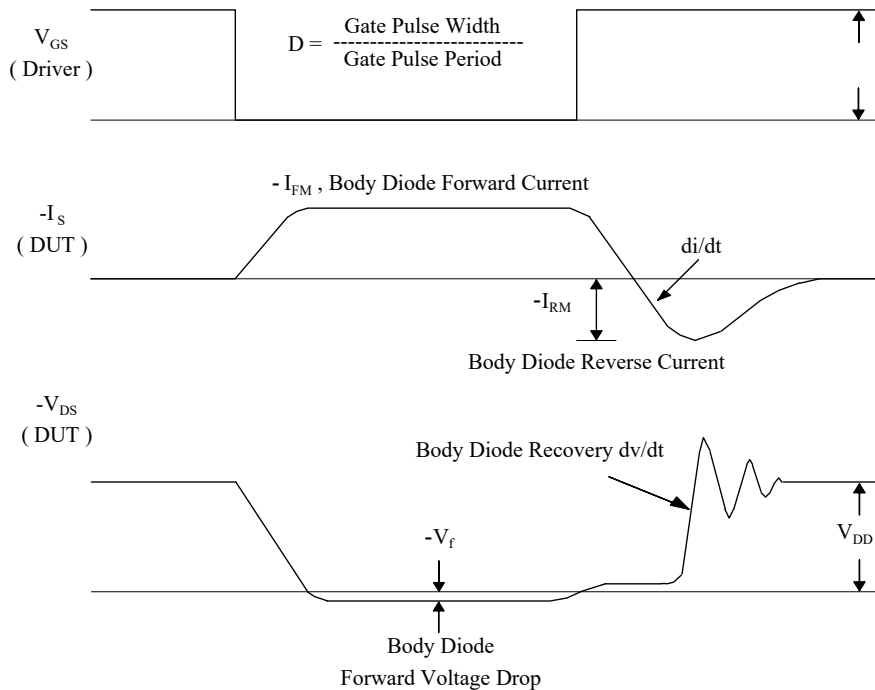
Unclamped Inductive Switching Test Circuit & Waveforms



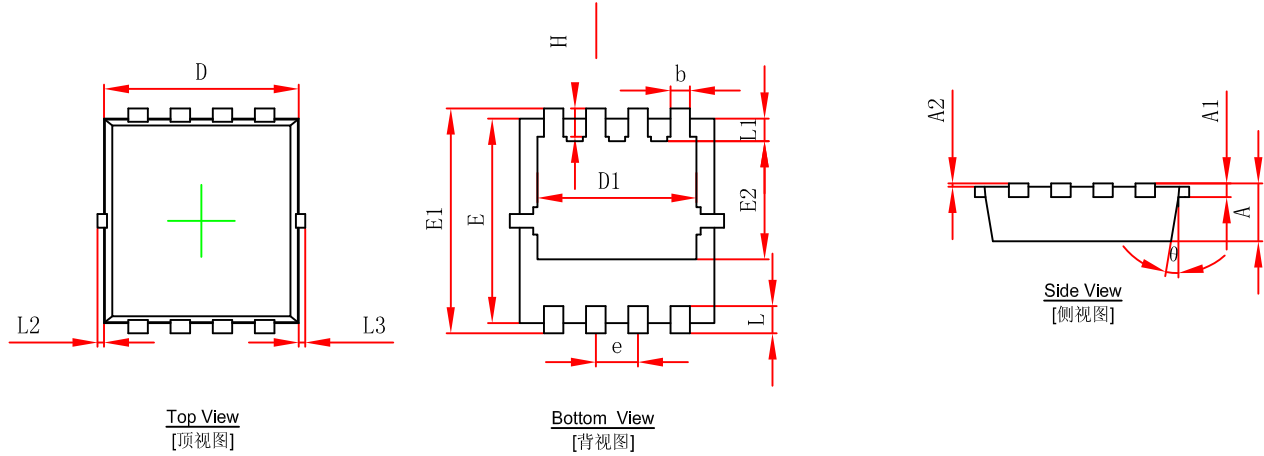
Peak Diode Recovery dv/dt Test Circuit & Waveforms



- dv/dt controlled by R_G
- I_{SD} controlled by pulse period

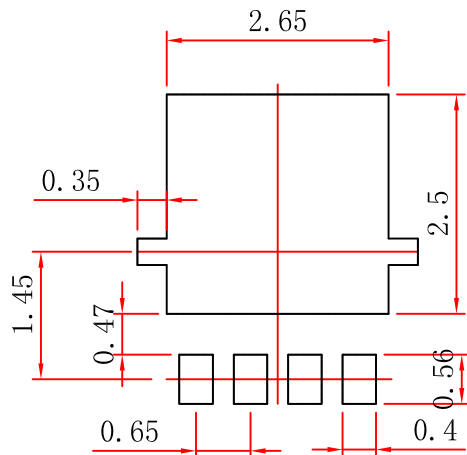


PDFNWB3.3x3.3-8L Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.650	0.850	0.026	0.033
A1	0.152 REF.		0.006 REF.	
A2	0~0.05		0~0.002	
D	2.900	3.100	0.114	0.122
D1	2.300	2.600	0.091	0.102
E	2.900	3.100	0.114	0.122
E1	3.150	3.450	0.124	0.136
E2	1.535	1.935	0.060	0.076
b	0.200	0.400	0.008	0.016
e	0.550	0.750	0.022	0.030
L	0.300	0.500	0.012	0.020
L1	0.180	0.480	0.007	0.019
L2	0~0.100		0~0.004	
L3	0~0.100		0~0.004	
H	0.315	0.515	0.012	0.020
θ	9°	13°	9°	13°

PDFNWB3.3x3.3-8L Suggested Pad Layout



Note:

1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.05\text{mm}$.
3. The pad layout is for reference purposes only.