

General Description

The TF070P03N combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$.

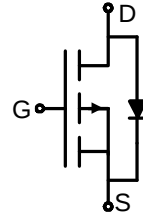
Features

Advance high cell density Trench technology
Low $R_{DS(ON)}$ to minimize conductive loss
Low Gate Charge for fast switching
Low Thermal resistance

Application

MB/VGA Vcore
SMPS 2nd Synchronous Rectifier
POL application
BLDC Motor driver

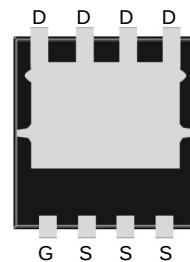
Product Summary



$$V_{DS} = -30V \quad I_D = -70A$$

$$R_{DS(ON)}(-10V \text{ typ}) = 7.5m\Omega$$

$$R_{DS(ON)}(-4.5V \text{ typ}) = 11m\Omega$$



PDFNWB5x6-8L

Ordering Information:

Part NO.	TF070P03N
Marking1	070P03N
Marking2	TF:tuofeng; Y:year code; X:Week; AA:device code;
Basic ordering unit (pcs)	5000

Absolute Maximum Ratings ($T_C = 25^\circ C$)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	$I_{D@T_C=25^\circ C}$	-70	A
	$I_{D@T_C=75^\circ C}$	-49	A
	$I_{D@T_C=100^\circ C}$	-42	A
Pulsed Drain Current ^①	I_{DM}	-230	A
Total Power Dissipation ^②	$P_D@T_C=25^\circ C$	60	W
Total Power Dissipation	$P_D@T_A=25^\circ C$	2.0	W
Operating Junction Temperature	T_J	-55 to 150	$^\circ C$
Storage Temperature	T_{STG}	-55 to 150	$^\circ C$

●Thermal resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance, junction - case ^②	R _{thJC}	-	-	3.5	° C/W
Thermal resistance, junction - ambient	R _{thJA}	-	-	50	° C/W
Soldering temperature, wavesoldering for 8s	T _{sold}	-	-	265	° C

●Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D = -250uA	-30			V
Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = -250uA	-1.0	-1.5	-2.0	V
Drain-Source Leakage Current	I _{DSS}	V _{DS} = -28V, V _{GS} = 0V			-1.0	uA
Gate- Source Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} = 0V			±100	nA
Static Drain-source On Resistance	R _{DS(ON)}	V _{GS} = -10V, I _D = -20A		7.5	9.0	mΩ
		V _{GS} = -4.5V, I _D = -15A		11	14	mΩ
Forward Transconductance	g _{FS}	V _{DS} = -10V, I _D = -10A		12		S
Source-drain voltage	V _{SD}	I _S = -20A		0.85	1.00	V

●Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Input capacitance	C _{iss}	f = 1MHz V _{DD} = -30V V _{GS} = 0V	-	2497	-	pF
Output capacitance	C _{oss}		-	240	-	
Reverse transfer capacitance	C _{rss}		-	230	-	

●Gate Charge characteristics(T_a = 25°C)

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Total gate charge	Q _g	V _{DD} = -15V I _D = -20A V _{GS} = -10V	-	32.0	-	nC
Gate - Source charge	Q _{gs}		-	6.60	-	
Gate - Drain charge	Q _{gd}		-	8.00	-	
Turn-On Delay Time	t _{d(on)}	V _{GS} = -10V V _{DD} = -15V R _L = 3.0Ω I _D = -30A	-	14.0	-	nS
Turn-On Rise Time	t _r		-	20.0	-	
Turn-Off Delay Time	t _{d(off)}		-	56.0	-	
Turn-Off Fall Time	t _f		-	48.0	-	

Note:

① Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2% ;

Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate;

P- Channel Typical Characteristics

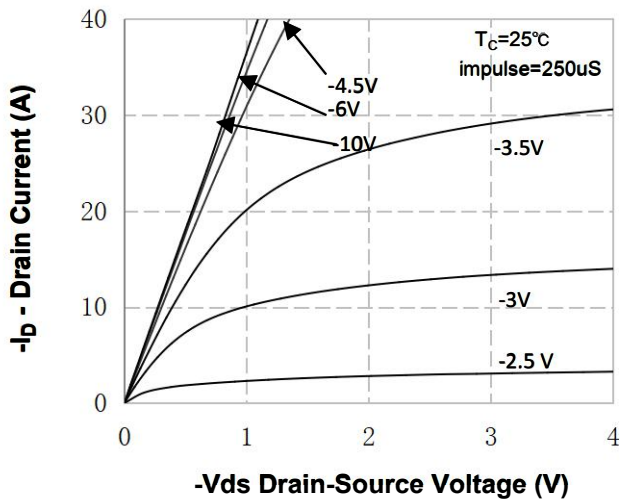


Figure 1. On-Region Characteristics

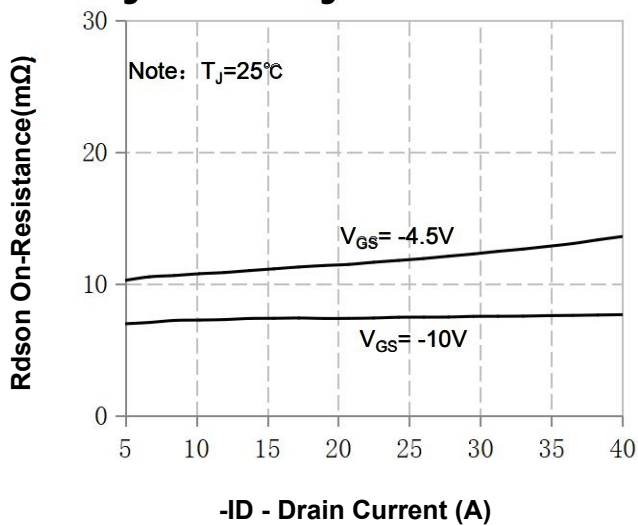


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

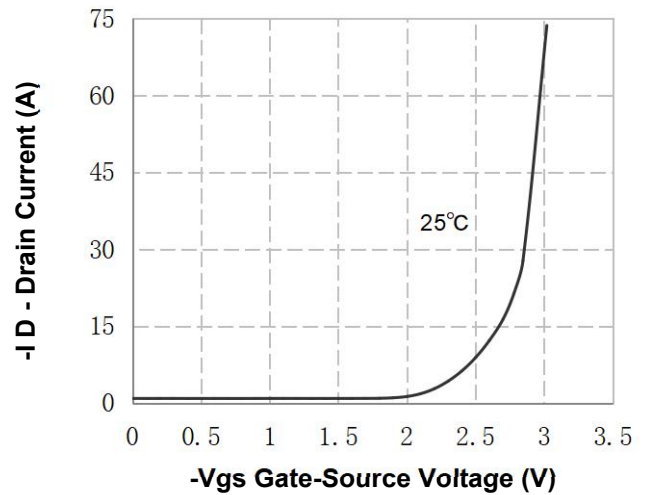


Figure 2. Transfer Characteristics

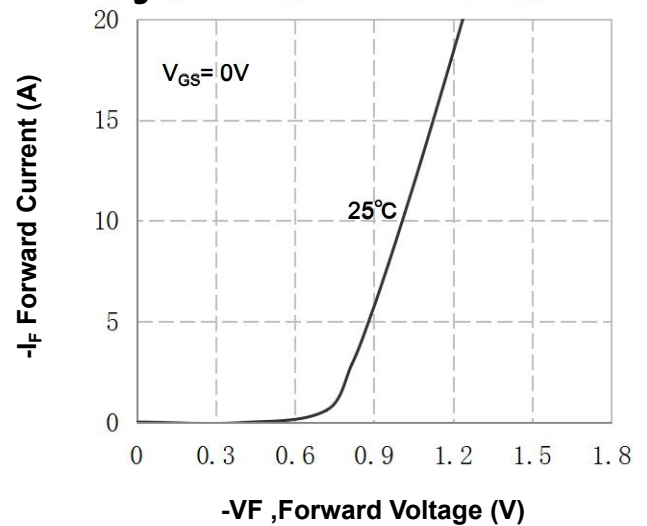


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

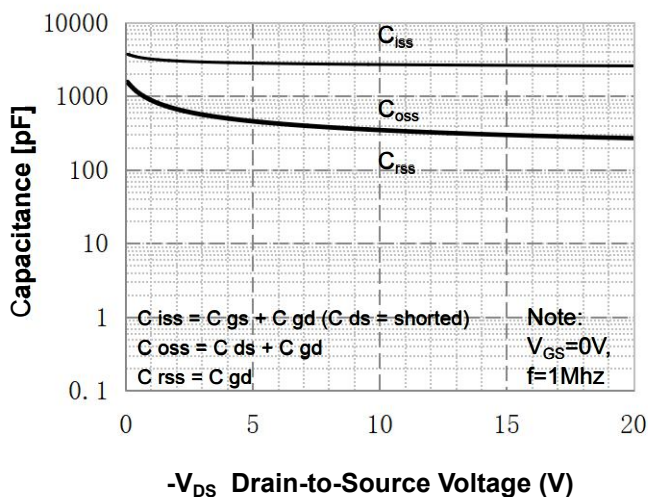


Figure 5. Capacitance Characteristics

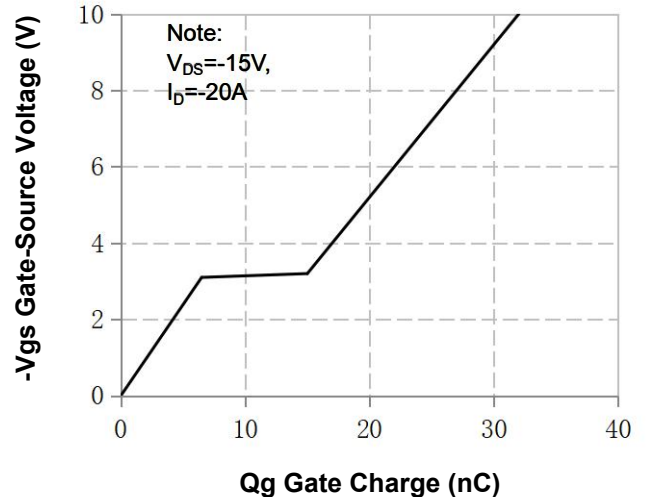


Figure 6. Gate Charge Characteristics

P- Channel Typical Characteristics (Continued)

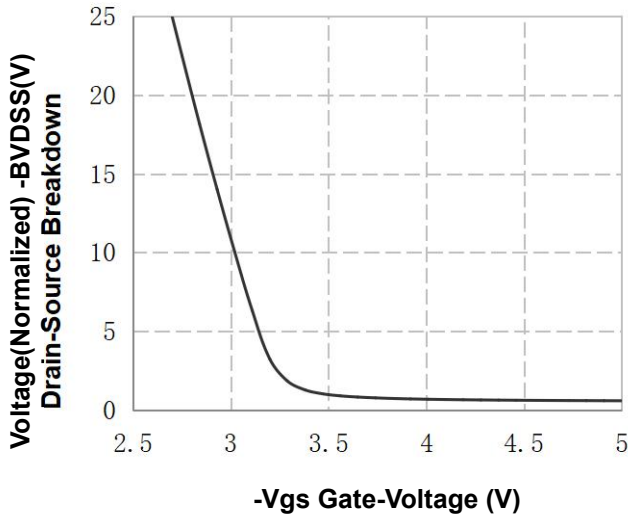


Figure 7. Breakdown Voltage Variation vs Gate-Voltage

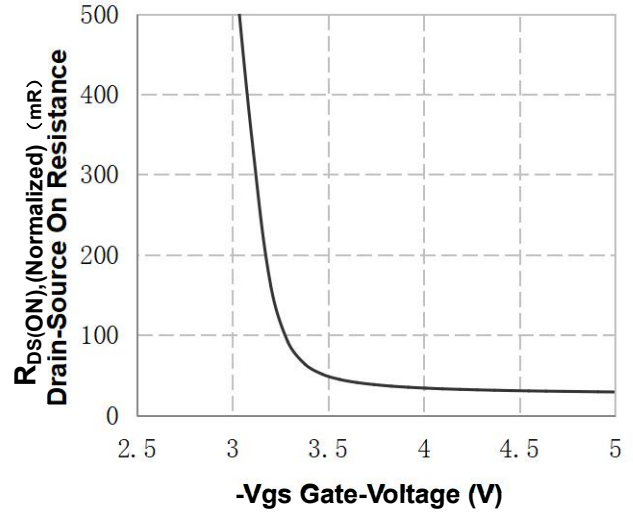


Figure 8. On-Resistance Variation vs Gate Voltage

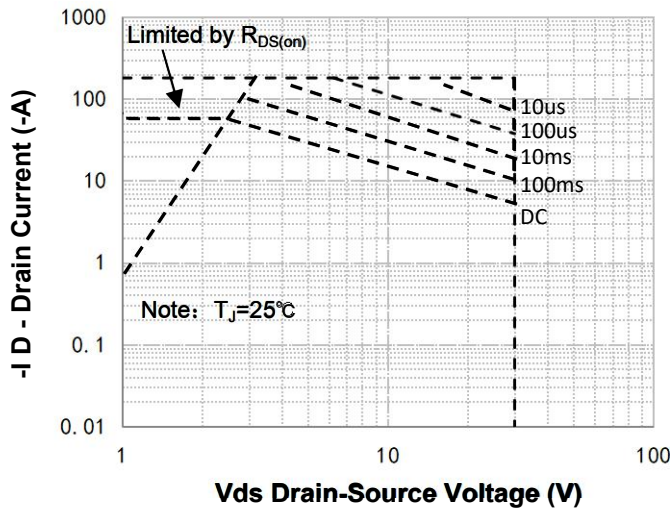


Figure 9. Maximum Safe Operating Area

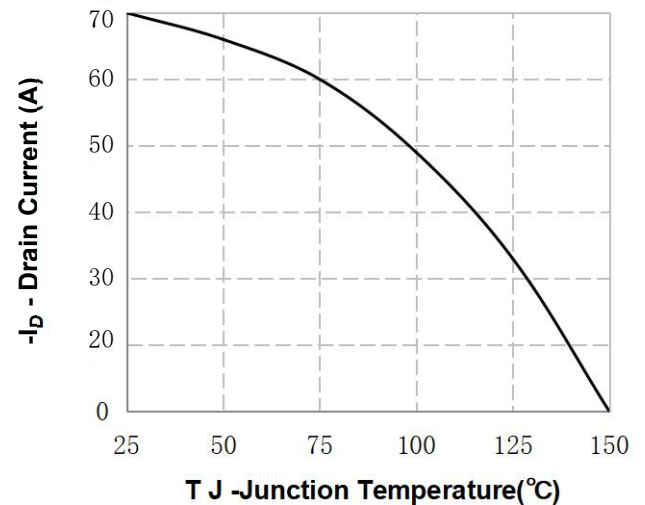


Figure 10. Maximum Continuous Drain Current vs Case Temperature

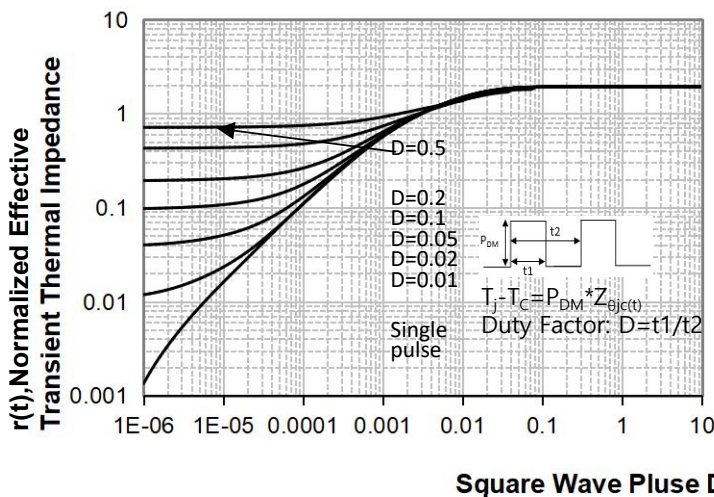
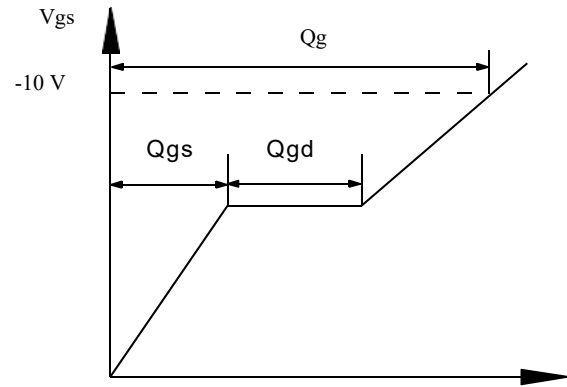
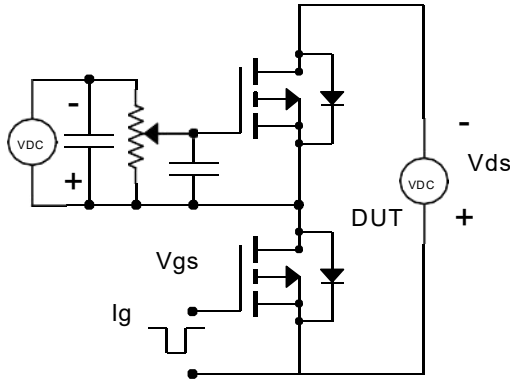
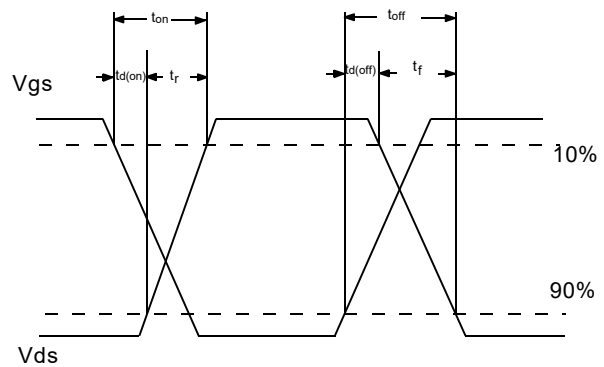
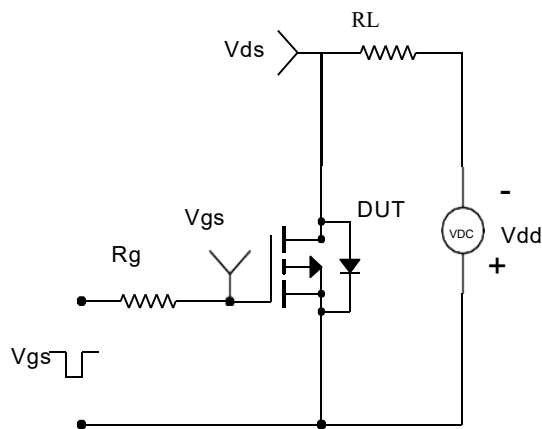


Figure 11. Transient Thermal Response Curve

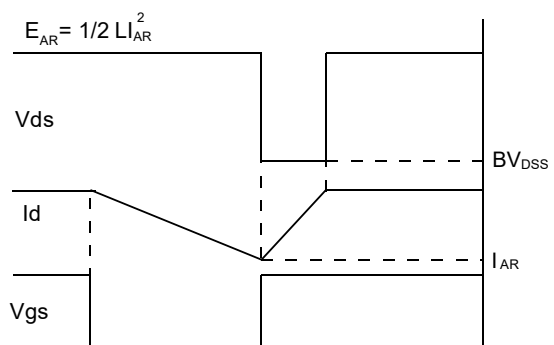
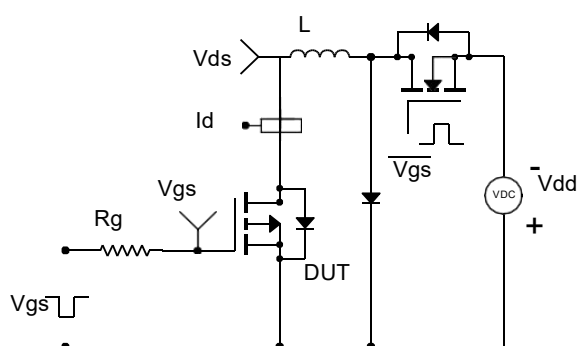
Gate Charge Test Circuit & Waveform



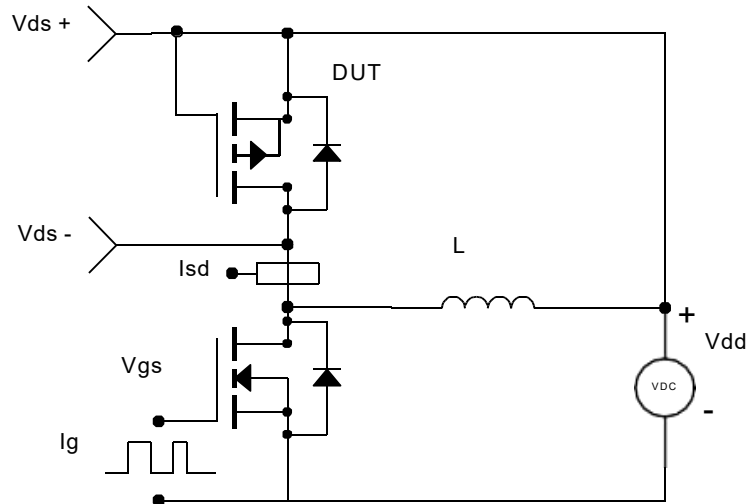
Resistive Switching Test Circuit & Waveforms



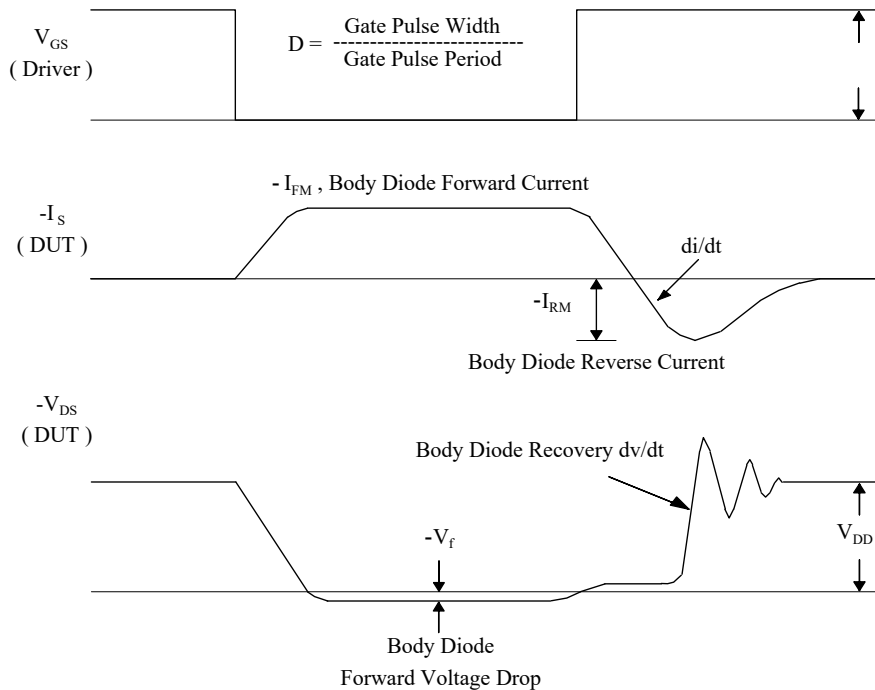
Unclamped Inductive Switching Test Circuit & Waveforms



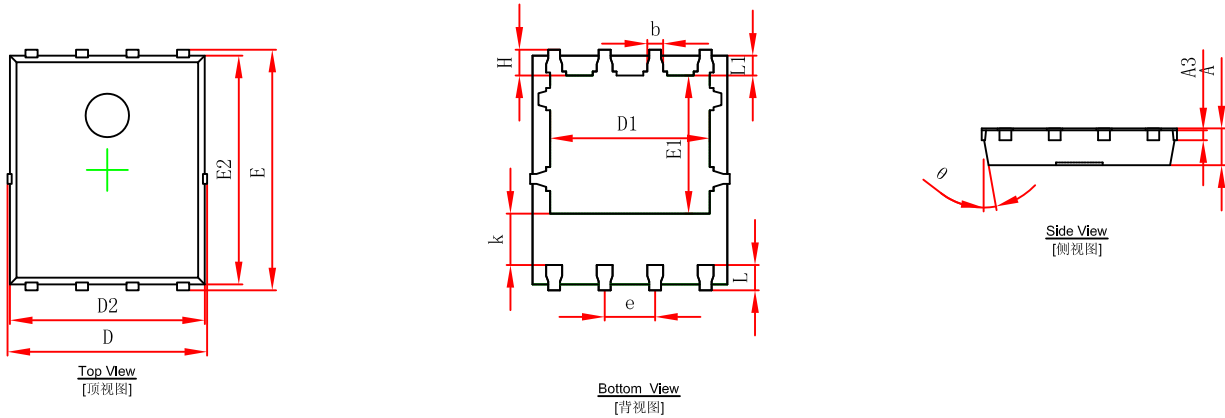
Peak Diode Recovery dv/dt Test Circuit & Waveforms



- dv/dt controlled by R_G
- I_{SD} controlled by pulse period

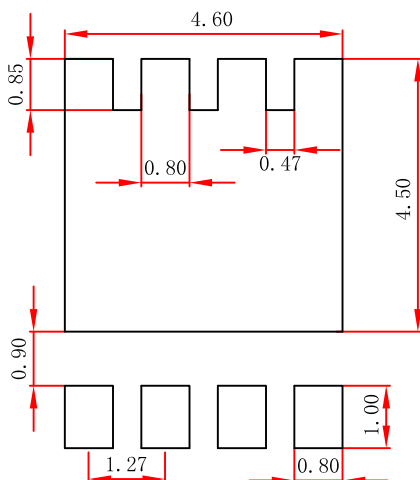


PDFNWB5x6-8L Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	10°	12°	10°	12°

PDFNWB5x6-8L Suggested Pad Layout



Note:
1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.05\text{mm}$.
3. The pad layout is for reference purposes only.