



SHENZHEN TUOFENG SEMICONDUCTOR TECHNOLOGY CO.,LTD

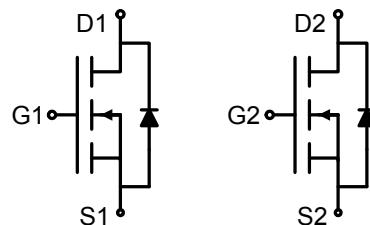
## N-CHANNEL ENHANCEMENT MODE POWER MOSFET

SGT MOS、低内阻、低结电容开关损耗小

TFD085N03MG

**Description**

The TFD085N03MG uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a battery protection or in other switching application.



Schematic diagram

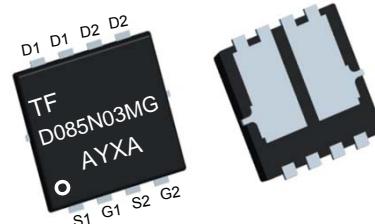
**General Feature** $V_{DS} = 30V$ ,  $I_D = 23A$  $R_{DS(ON)\text{ Typ}} = 8.7m\Omega$  @  $V_{GS}=10V$  $R_{DS(ON)\text{ Typ}} = 12m\Omega$  @  $V_{GS}=4.5V$ High Power and current handing capability  
Lead free product is acquired

Surface mount package

**Application**

Battery switch

DC/DC converter



PDFN3333-8

**• Package Marking and Ordering Information:**

Part NO.	TFD085N03MG
Marking1	D085N03MG:TFD085N03MG
Marking2	TF:tuofeng; Y:year code; X:Week; AA:device code;
Basic ordering unit (pcs)	5000

**• Absolute Maximum Ratings ( $T_C = 25^\circ C$ )**

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	$V_{DS}$	30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current	$I_D@TC=25^\circ C$	23	A
	$I_D@TC=75^\circ C$	16	A
	$I_D@TC=100^\circ C$	13	A
Pulsed Drain Current <sup>①</sup>	$I_{DM}$	70	A
Total Power Dissipation	$P_D@TC=25^\circ C$	15	W
Total Power Dissipation	$P_D@TA=25^\circ C$	0.9	W
Operating Junction Temperature	$T_J$	-55 to 150	$^\circ C$
Storage Temperature	$T_{STG}$	-55 to 150	$^\circ C$
Single Pulse Avalanche Energy	$E_{AS}$	23	mJ



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## •Thermal resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance, junction - case	R <sub>thJC</sub>	-	-	8.0	° C/W
Thermal resistance, junction - ambient	R <sub>thJA</sub>	-	-	65	° C/W
Soldering temperature, wavesoldering for 8 s	T <sub>sold</sub>	-	-	265	° C

•Electronic Characteristics(T<sub>j</sub>=25 °C, unless otherwise note)

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	30	-	-	V
Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250uA	1.1	1.4	2.0	V
Drain-Source Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> =30 V <sub>GS</sub> =0V	-	-	1.0	uA
Gate- Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V ,V <sub>DS</sub> =0V	-	-	±100	nA
Static Drain-source On Resistance	R <sub>DSS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =10A	-	8.7	10	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =8.0A	-	12	15	mΩ
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =25V, I <sub>D</sub> =10A	-	8	-	S
Source-drain voltage	V <sub>SD</sub>	I <sub>S</sub> =10A	-	-	1.20	V

## •Electronic Characteristics

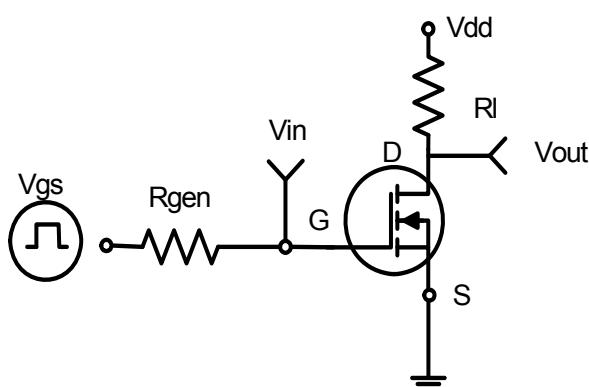
Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Input capacitance	C <sub>iss</sub>	f = 1MHz V <sub>DS</sub> =15V V <sub>GS</sub> =0V	-	375.0	-	pF
Output capacitance	C <sub>oss</sub>		-	160.0	-	
Reverse transfer capacitance	C <sub>rss</sub>		-	19.0	-	

•Gate Charge characteristics(T<sub>a</sub> = 25°C)

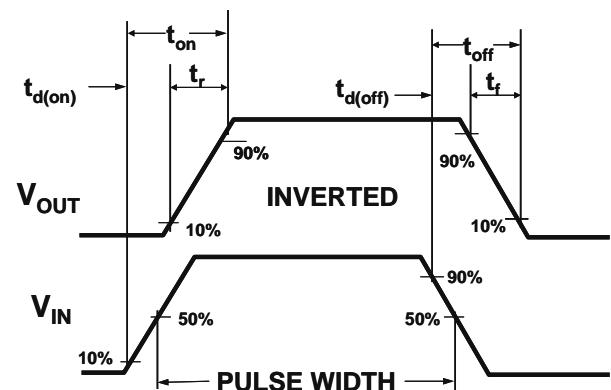
Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Total gate charge	Q <sub>g</sub>	V <sub>DD</sub> = 15V ID = 10A V <sub>GS</sub> = 10V	-	8.30	-	nC
Gate - Source charge	Q <sub>gs</sub>		-	1.90	-	
Gate - Drain charge	Q <sub>gd</sub>		-	1.60	-	

Note: ① Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2% ;

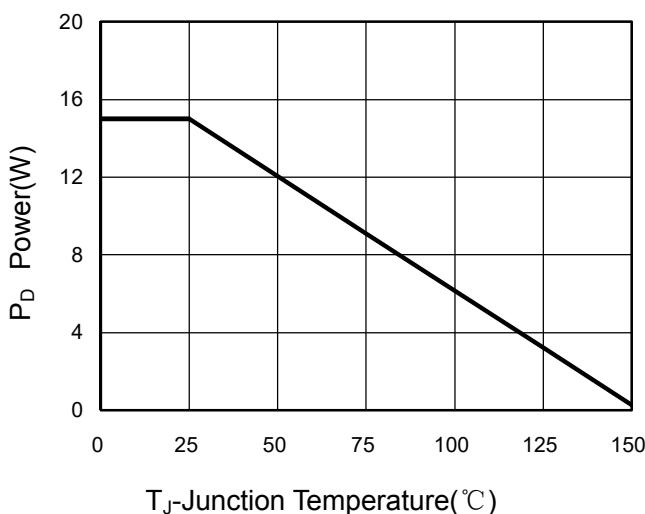
**Typical Electrical and Thermal Characteristics**



**Figure 1 Switching Test Circuit**

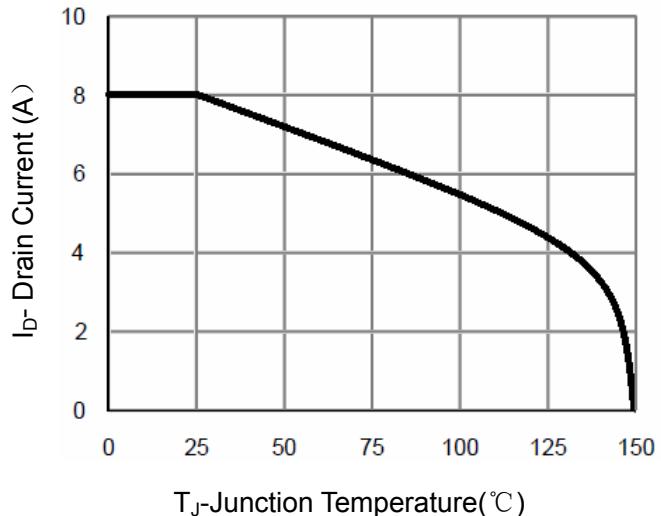


**Figure 2 Switching Waveforms**



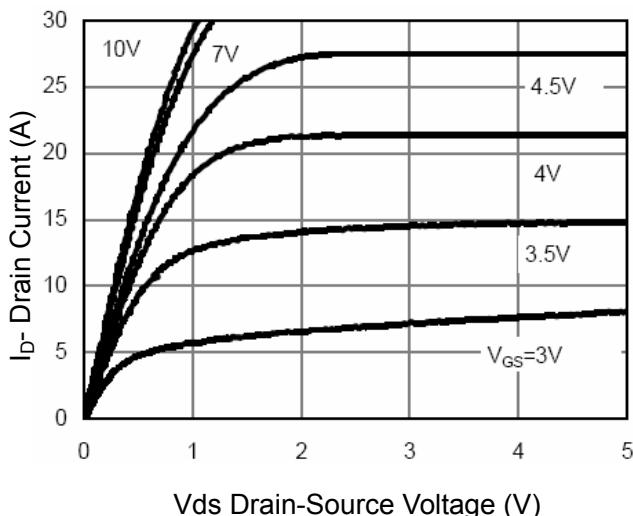
T<sub>j</sub>-Junction Temperature(°C)

**Figure 3 Power Dissipation**



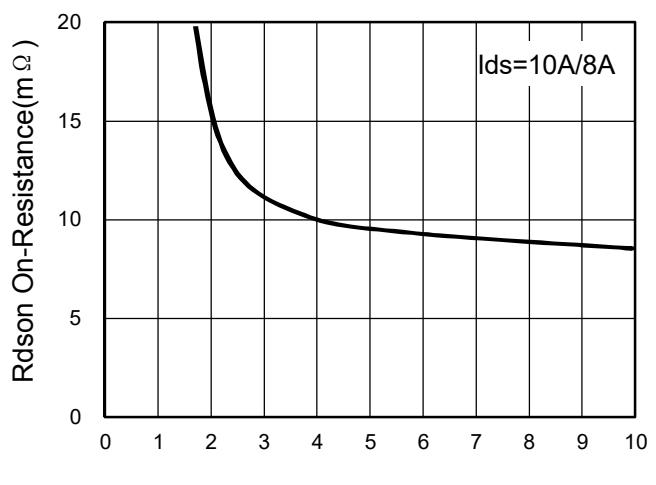
T<sub>j</sub>-Junction Temperature(°C)

**Figure 4 Drain Current**



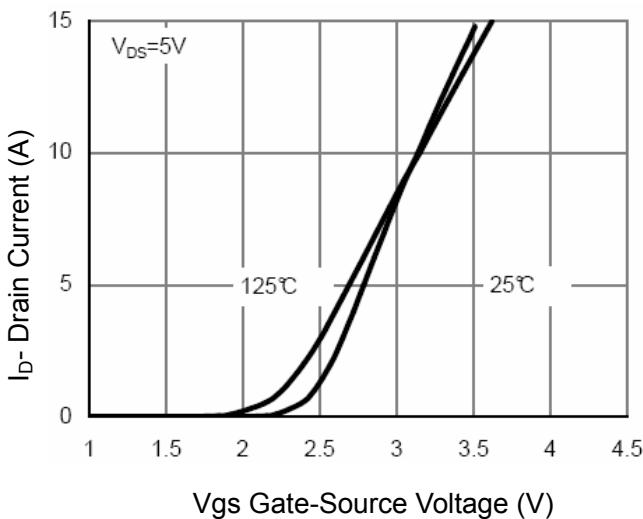
Vds Drain-Source Voltage (V)

**Figure 5 Output Characteristics**

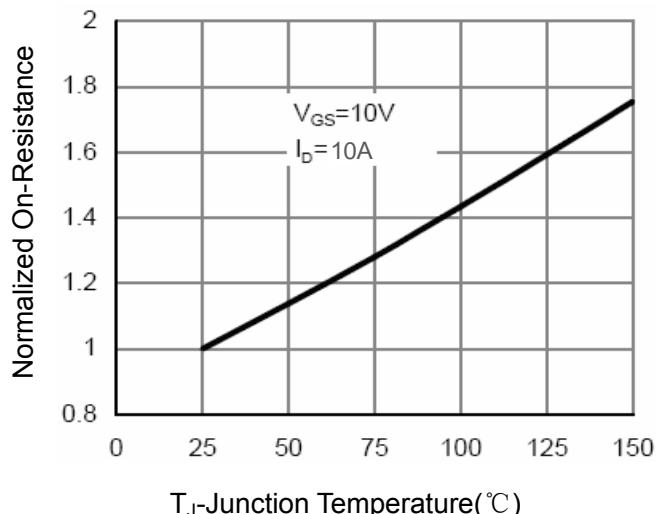


I<sub>d</sub>- Drain Current (A)

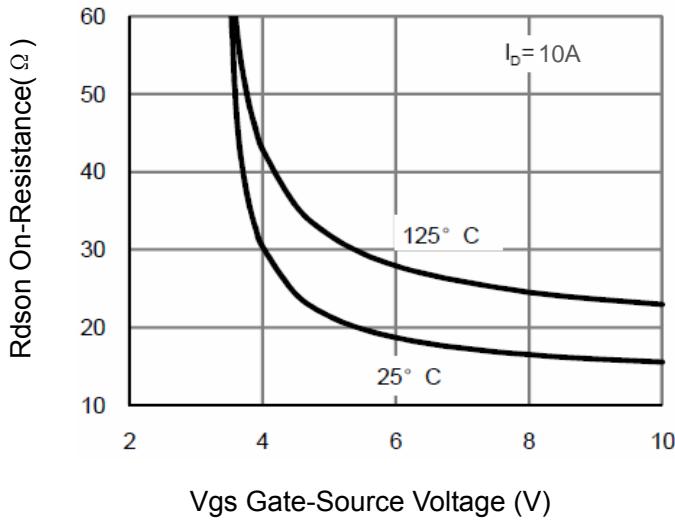
**Figure 6 Drain-Source On-Resistance**



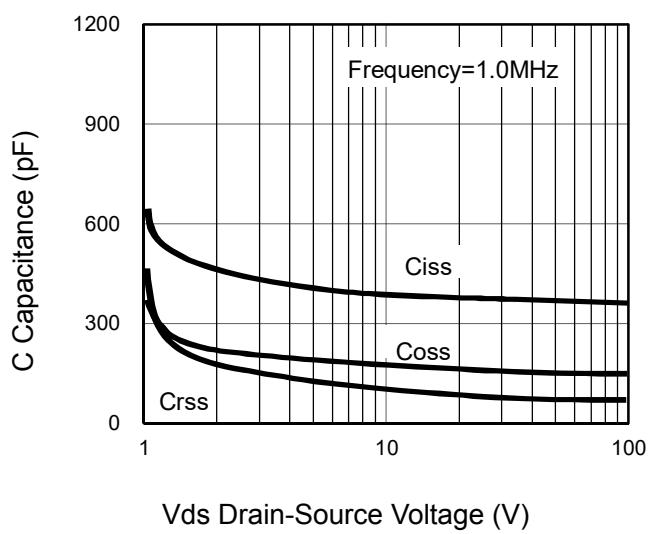
**Figure 7 Transfer Characteristics**



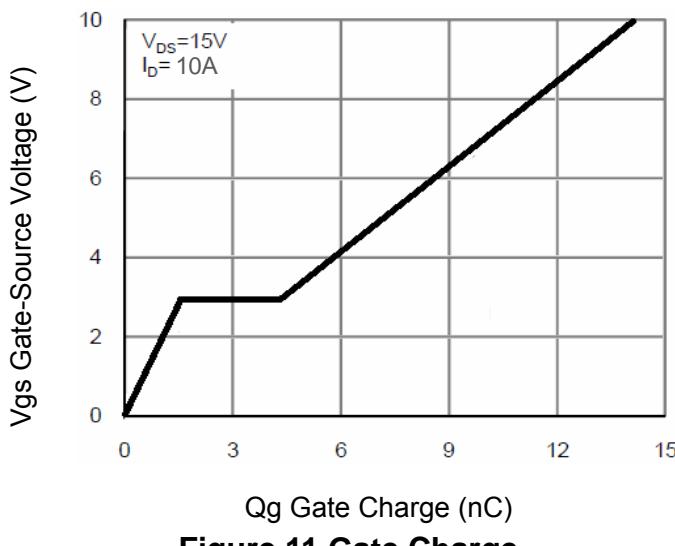
**Figure 8 Drain-Source On-Resistance**



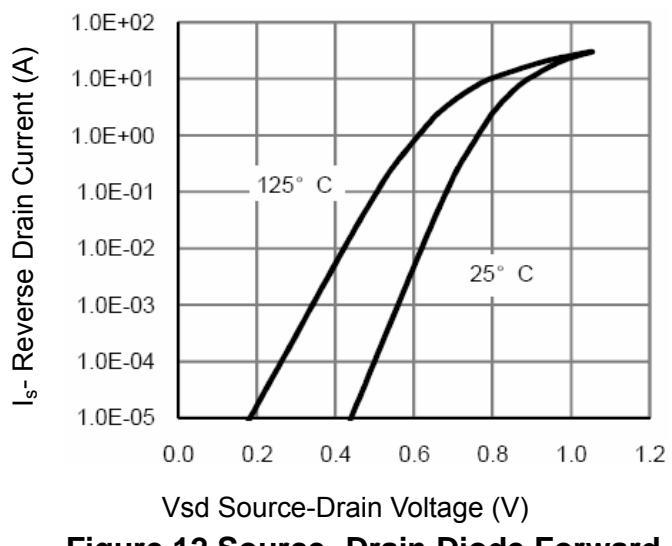
**Figure 9  $R_{DS(on)}$  vs  $V_{GS}$**



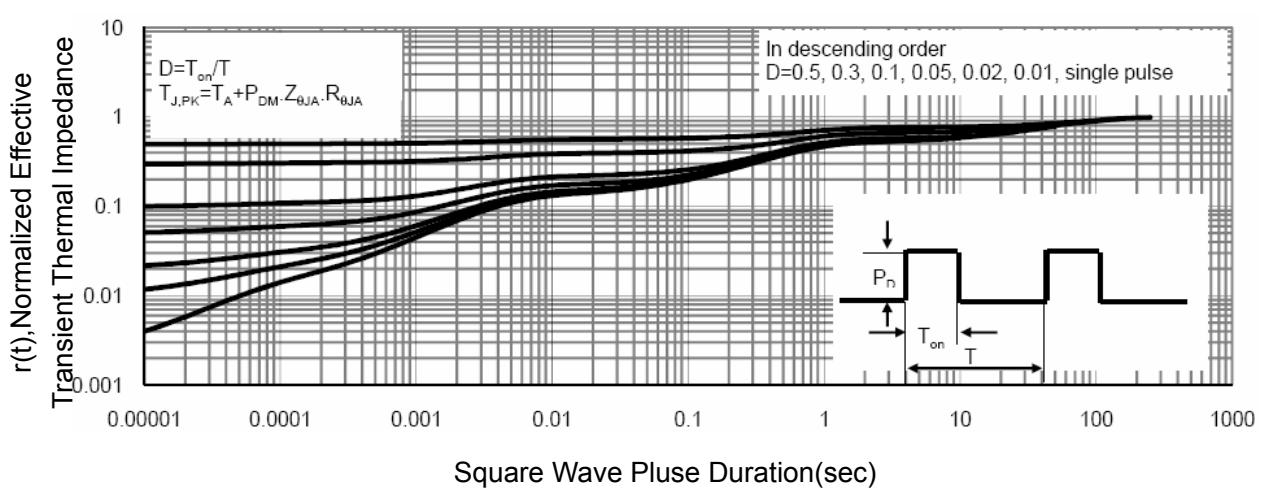
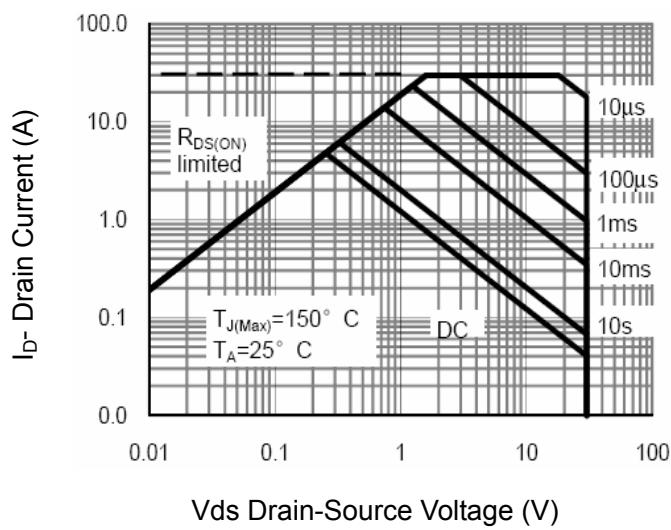
**Figure 10 Capacitance vs  $V_{DS}$**



**Figure 11 Gate Charge**



**Figure 12 Source-Drain Diode Forward**





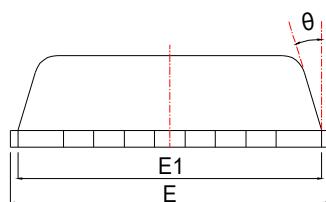
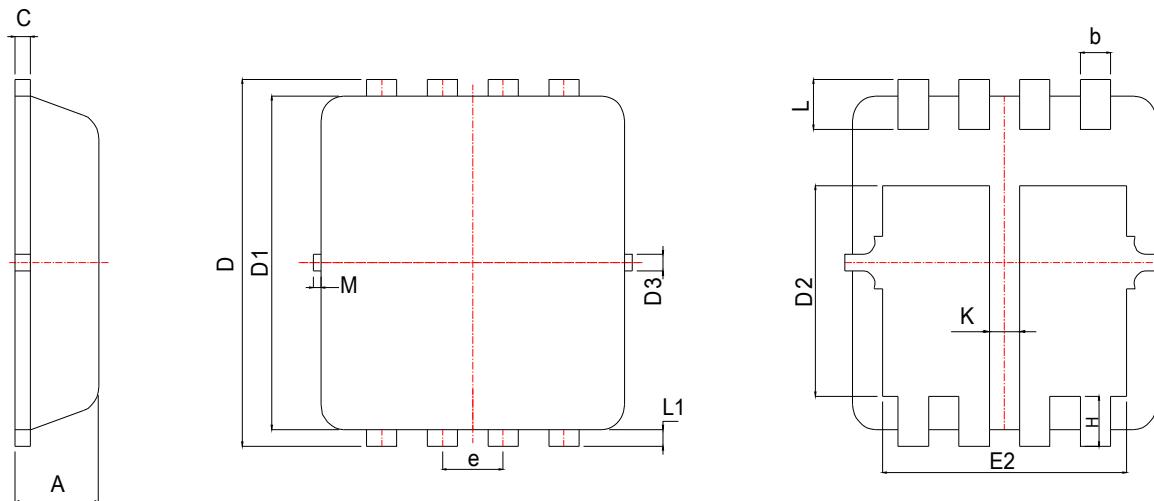
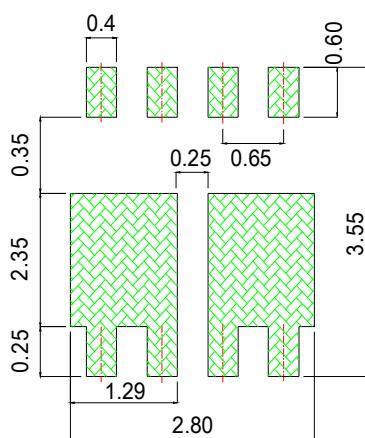
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PDFN3333-8L

Land Pattern  
(Only for Reference)

SYMBOL	MM			INCH			SYMBOL	MM			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX		MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.031	E1	3.00	3.15	3.20	0.118	0.122	0.126
b	0.25	0.30	0.35	0.010	0.012	0.014	E2	2.39	2.49	2.59	0.094	0.098	0.102
c	0.10	0.15	0.25	0.004	0.007	0.010	e	0.65BSC			0.026BSC		
D	3.25	3.35	3.45	0.128	0.132	0.136	H	0.30	0.40	0.50	0.012	0.016	0.020
D1	3.00	3.10	3.20	0.118	0.122	0.126	L	0.30	0.40	0.50	0.012	0.016	0.020
D2	1.78	1.88	1.98	0.070	0.074	0.078	L1	*	0.13	*	*	0.005	*
D3	*	0.13	*	*	0.005	*	M	*	*	0.15	*	*	0.006
E	3.20	3.30	3.40	0.126	0.130	0.134	θ	10°	12°	*	10°	12°	
K	0.30	*	*	0.012	*	*							