P -CHANNEL ENHANCEMENT MODE POWER MOSFET

TF060P03M

● General Description

The TF060P03M combines advanced trench MOSFETtechnology with a low resistance package toprovide extremely low $R_{DS(ON)}$.

● Features

Advance high cell density Trench technology

Low $R_{DS(ON)}$ to minimize conductive loss

Low Gate Charge for fast switching

Low Thermal resistance

●Application

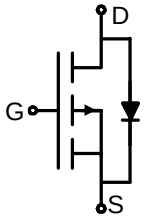
MB/VGA Vcore

SMPS 2nd Synchronous Rectifier

POL application

BLDC Motor driver

● Product Summary

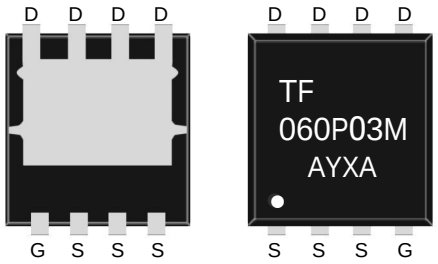


V_{DS} =-30V I_D=-70A

$R_{DSON(-10V\ typ)}$ =5.7mΩ

$R_{DSON(-4.5V\ typ)}$ =7.8mΩ

RoHS compliant



PDFN3333-8L

●Ordering Information:

Part NO.	TF060P03M
Marking1	TF060P03M
Marking2	TF:tuofeng; Y:year code; X:Week; AA:device code;
Basic ordering unit (pcs)	5000

●Absolute Maximum Ratings (T_C =25℃)

Parameter	**Symbol**	Rating	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current	$I_{D@}T_C$=25℃	-70	A
	$I_{D@}T_C$=75℃	-49	A
	$I_{D\ @}T_C$=100℃	-42	A
Pulsed Drain Current ①	I_{DM}	-190	A
Total Power Dissipation②	$P_D@T_C$=25℃	65	W
Total Power Dissipation	$P_D@T_A$=25℃	2.0	W
Operating Junction Temperature	T_J	-55 to 150	℃
Storage Temperature	T_{STG}	-55 to 150	℃

●Thermal resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance, junction - case②	R_{thJC}	-	-	4.2	° C/W
Thermal resistance, junction - ambient	R_{thJA}	-	-	55	° C/W
Soldering temperature, wavesoldering for 8s	T_{sold}	-	-	265	° C

●Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} =0V, I_D =-250uA	-30			V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} =V_{DS}, I_D =-250uA	-1.0	-1.6	-2.0	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=-28V, V_{GS} =0V			-1.0	uA
Gate- Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS} =0V			±100	nA
Static Drain-source On Resistance	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-20A		5.7	7.0	mΩ
		V_{GS}=-4.5V, I_D=-10A		7.8	9.5	mΩ
Forward Transconductance	g_{FS}	V_{DS} =-10V, I_D=-10A		12		S
Source-drain voltage	V_{SD}	Is=-20A		0.85	1.00	V

●Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Input capacitance	C_{iss}	f = 1MHz V_{DD} = -15V V_{GS} = 0V	-	3151	-	pF
Output capacitance	C_{oss}		-	359	-	
Reverse transfer capacitance	C_{rss}		-	343	-	

●Gate Charge characteristics(T_a = 25℃)

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Total gate charge	Q_g	V_{DD} = -15V I_D = -20A V_{GS} = -10V	-	85.0	-	nC
Gate - Source charge	Q_{gs}		-	14.0	-	
Gate - Drain charge	Q_{gd}		-	16.0	-	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = -15V V_{GS} = -10V R_L = 3Ω I_D = -20A	-	11.0	-	ns
Turn-On Rise Time	t_r		-	48.0	-	ns
Turn-Off Delay Time	$t_{d(off)}$		-	76.0	-	ns
Turn-Off Fall Time	t_f		-	45.0	-	ns

Note:
① Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2% ;
② Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate;

P- Channel Typical Characteristics (Continued)

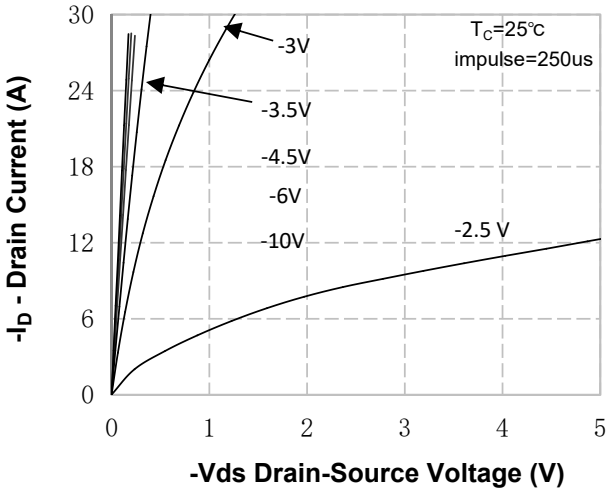


Figure 1. On-Region Characteristics

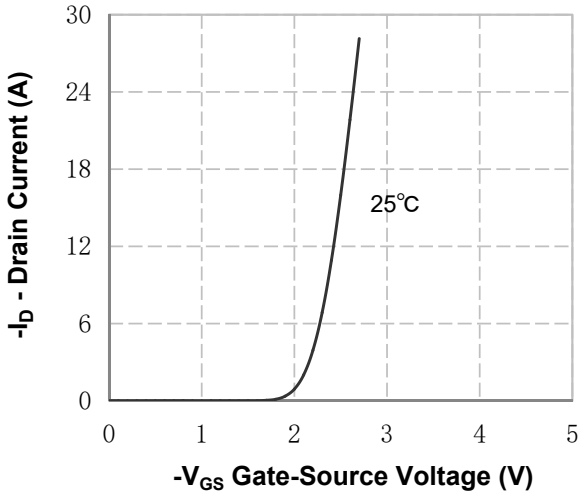


Figure 2. Transfer Characteristics

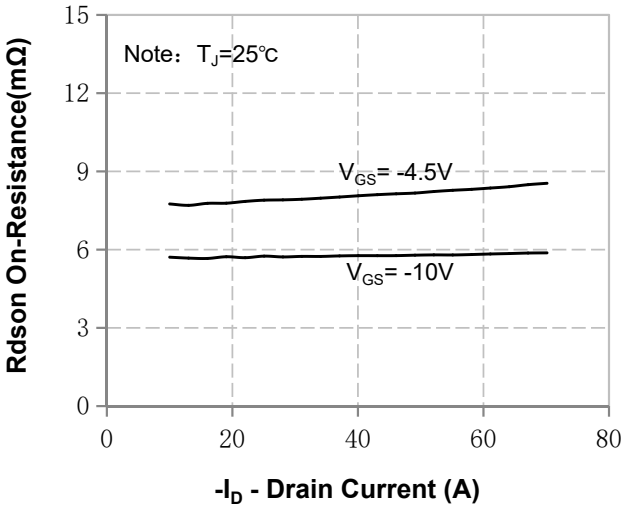


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

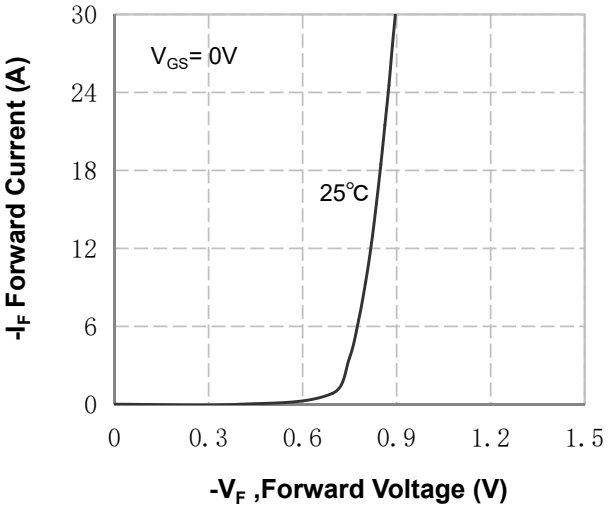


Figure 4. Body Diode Forward Voltage Variation with Source Current

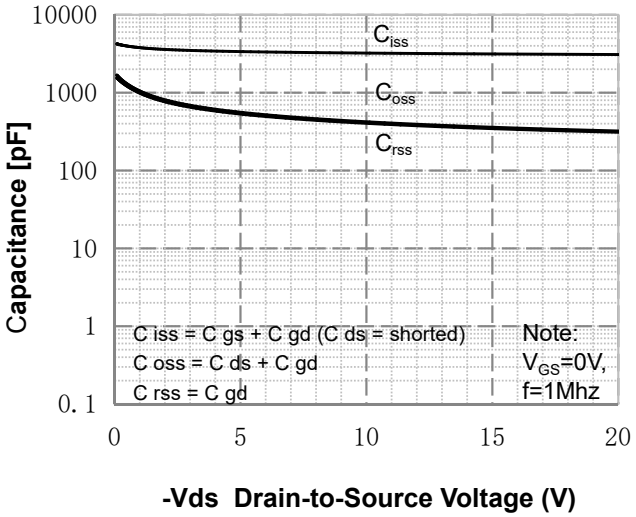


Figure 5. Capacitance Characteristics

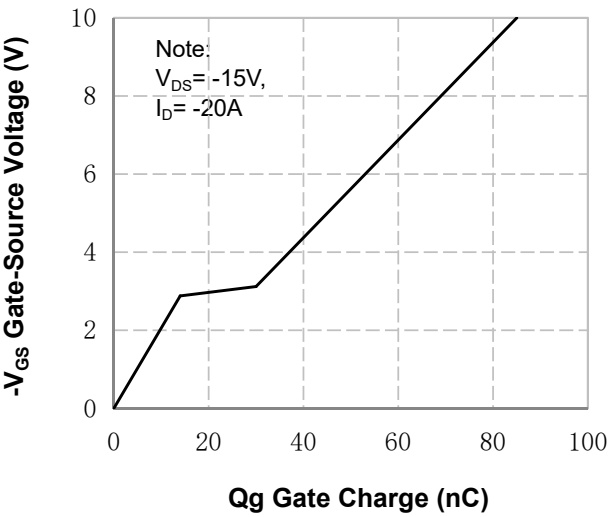


Figure 6. Gate Charge Characteristics

P- Channel Typical Characteristics (Continued)

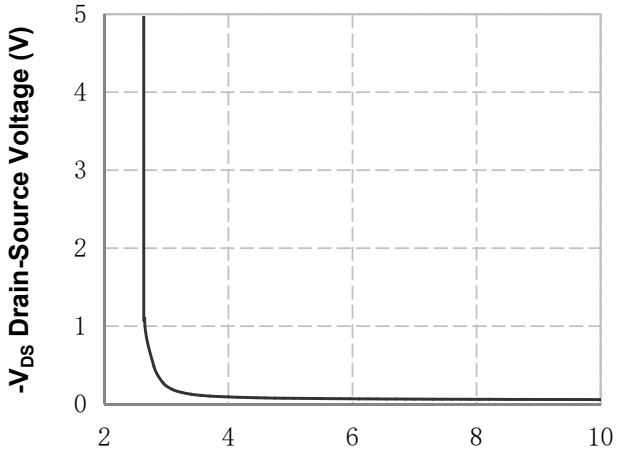


Figure 7. Vds Drain-Source Voltage vs Gate Voltage

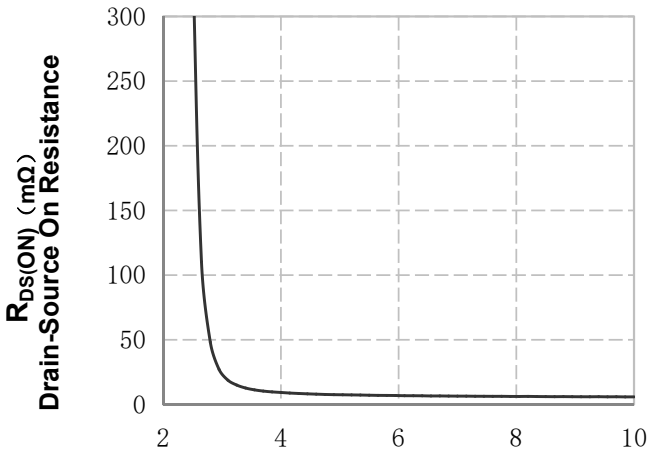


Figure 8. On-Resistance vs Gate Voltage

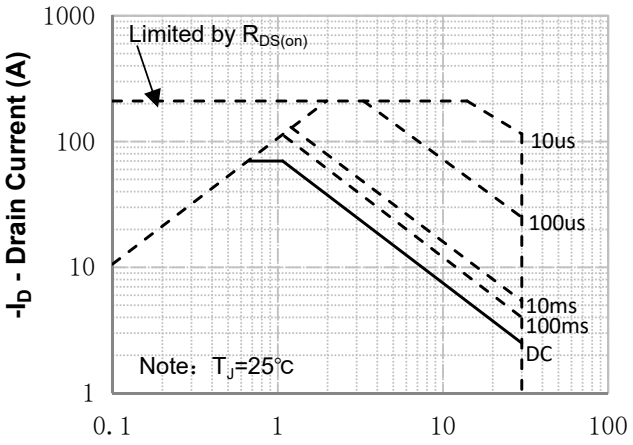


Figure 9. Maximum Safe Operating Area

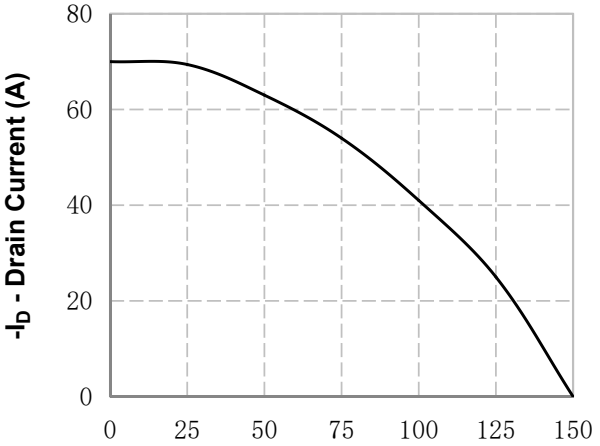


Figure 10. Maximum Continuous Drain Current vs Temperature

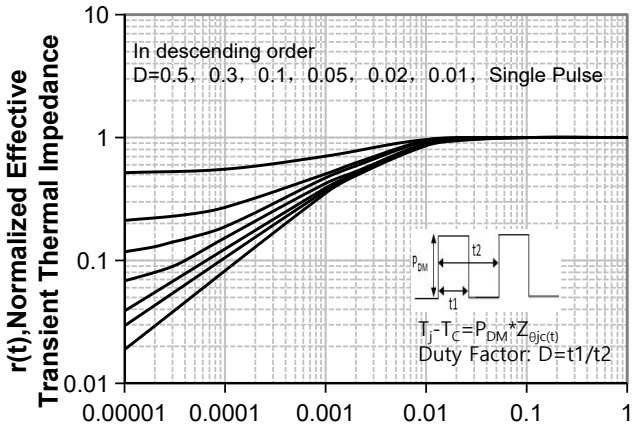
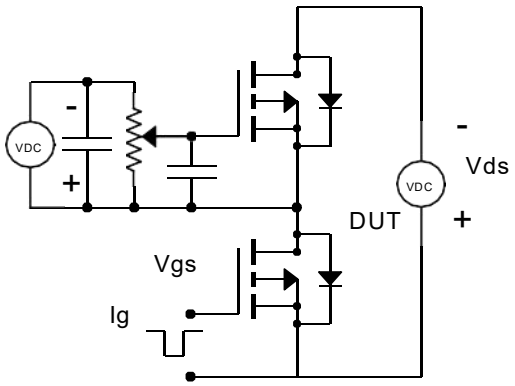
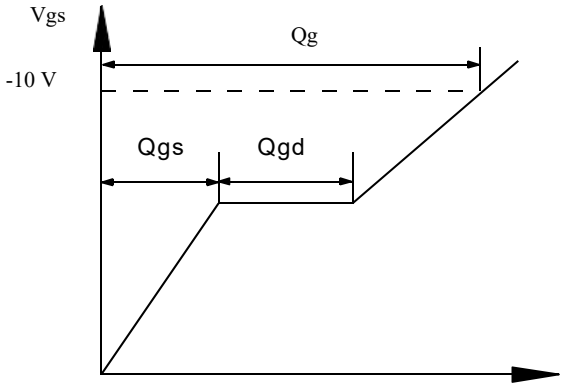


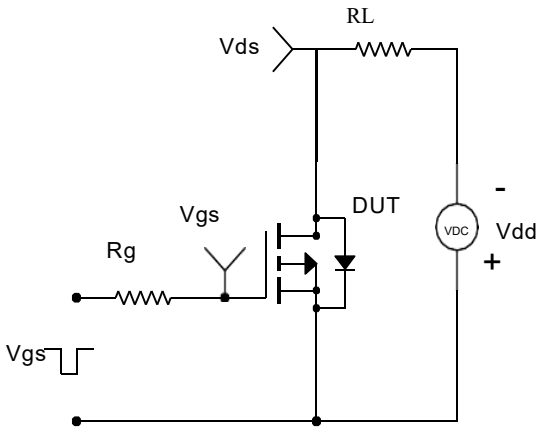
Figure 11. Transient Thermal Response Curve

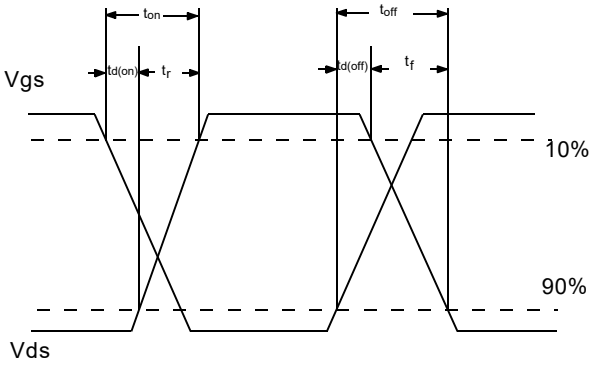
Gate Charge Test Circuit & Waveform



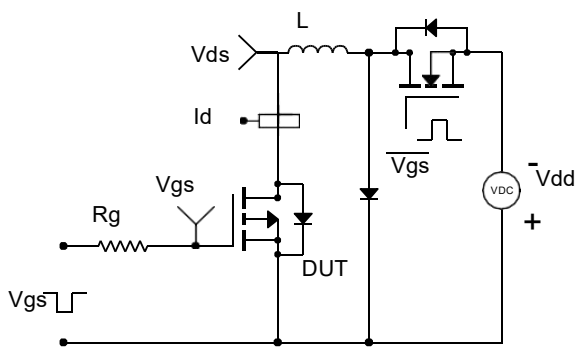


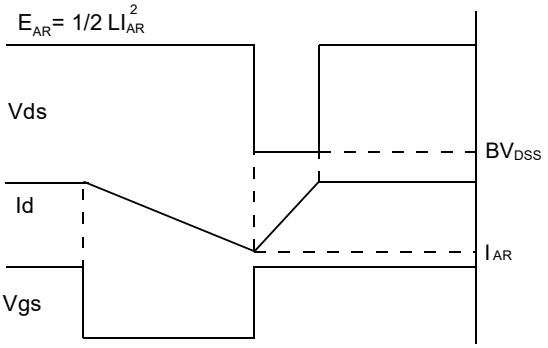
Resistive Switching Test Circuit & Waveforms



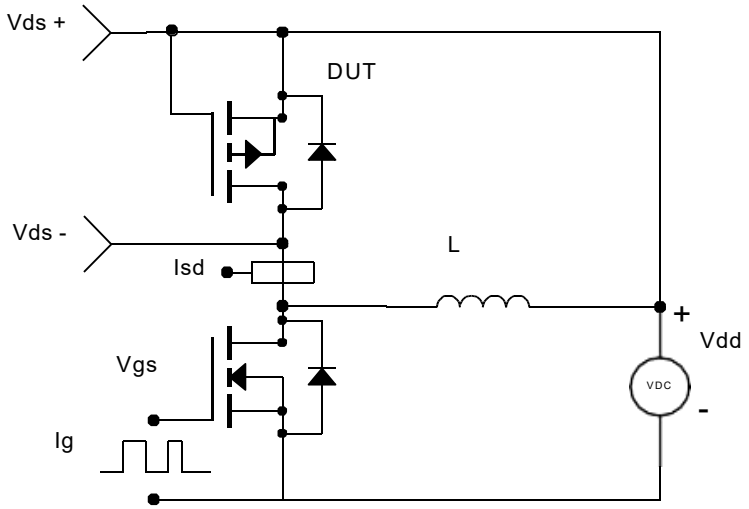


Unclamped Inductive Switching Test Circuit & Waveforms

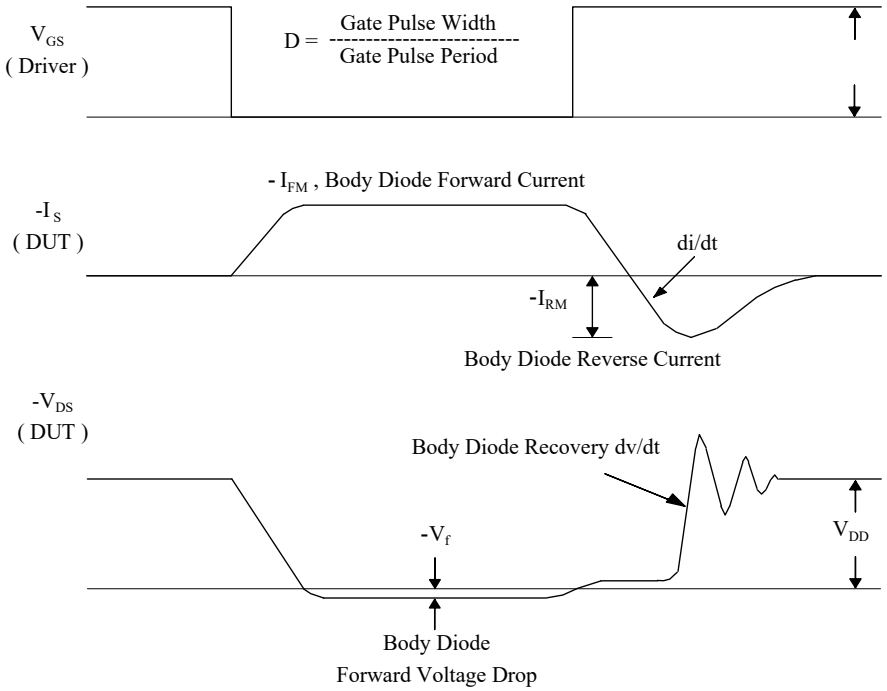




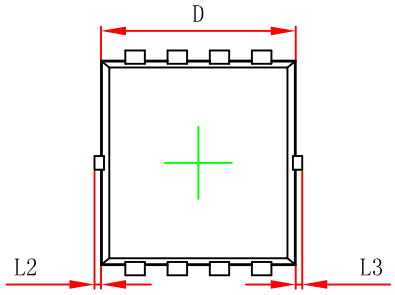
Peak Diode Recovery dv/dt Test Circuit & Waveforms



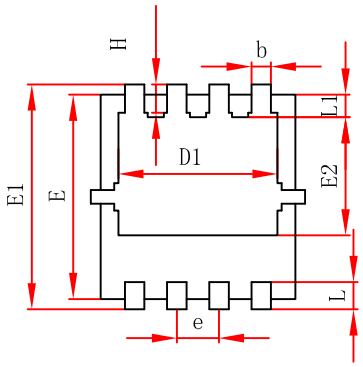
• dv/dt controlled by R_G
• I_{SD} controlled by pulse period



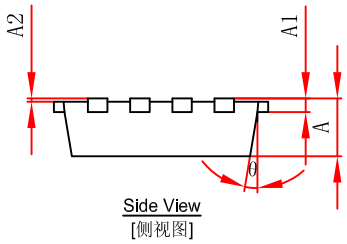
PDFN3333-8L Package Outline Dimensions



Top View
[顶视图]



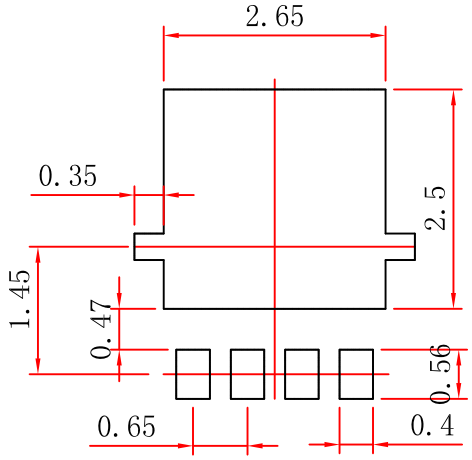
Bottom View
[背视图]



Side View
[侧视图]

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.650	0.850	0.026	0.033
A1	0.152 REF.		0.006 REF.	
A2	0~0.05		0~0.002	
D	2.900	3.100	0.114	0.122
D1	2.300	2.600	0.091	0.102
E	2.900	3.100	0.114	0.122
E1	3.150	3.450	0.124	0.136
E2	1.535	1.935	0.060	0.076
b	0.200	0.400	0.008	0.016
e	0.550	0.750	0.022	0.030
L	0.300	0.500	0.012	0.020
L1	0.180	0.480	0.007	0.019
L2	0~0.100		0~0.004	
L3	0~0.100		0~0.004	
H	0.315	0.515	0.012	0.020
θ	9°	13°	9°	13°

PDFN3333-8L Suggested Pad Layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.05mm.
3.The pad layout is for reference purposes only.