N-CHANNEL ENHANCEMENT MODE POWER MOSFET

TF025N02M

● General Description

The TF025N02M combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$.

● Features

Advance high cell density Trench technology

Low $R_{DS(ON)}$ to minimize conductive loss

Low Gate Charge for fast switching

Low Thermal resistance

●Application

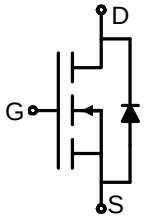
MB/VGA Vcore

SMPS 2nd Synchronous Rectifier

POL application

BLDC Motor driver

● Product Summary

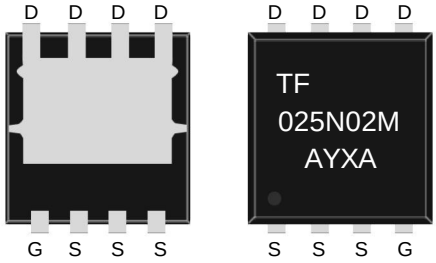


V_{DS} =20V I_D=90A

$R_{DSON(4.5V\ typ)}$=2.2mΩ

$R_{DSON(2.5V\ typ)}$=2.9mΩ

RoHS compliant



PDFN3333-8L

●Ordering Information:

Part NO.	TF025N02M
Marking1	025N02M:TF025N02M
Marking2	TF:tuofeng; Y:year code; X:Week; AA:device code;
Basic ordering unit (pcs)	5000

●Absolute Maximum Ratings (Tj=25℃,unless otherwise notse)

Parameter	**Symbol**	Rating	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	±12	V
Continuous Drain Current	$I_{D@}T_C$=25℃	90	A
	$I_{D@}T_C$=75℃	63	A
	$I_{D\ @}T_C$=100℃	54	A
Pulsed Drain Current ①	I_{DM}	260	A
Total Power Dissipation②	$P_D@T_C$=25℃	45	W
Total Power Dissipation	$P_D@T_A$=25℃	1.0	W
Operating Junction Temperature	T_J	-55 to 150	℃
Storage Temperature	T_{STG}	-55 to 150	℃

●Thermal resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance, junction - case②	R_{thJC}	-	-	2.0	°C/W
Thermal resistance, junction - ambient	R_{thJA}	-	-	50	°C/W
Soldering temperature, wavesoldering for 8s	T_{sold}	-	-	265	°C

●Electronic Characteristics(Tj=25℃,unless otherwise notse)

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} =0V, I_D =250uA	20			V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} =V_{DS}, I_D =250uA	0.5	0.7	1.2	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=20V, V_{GS} =0V			1.0	uA
Gate- Source Leakage Current	I_{GSS}	V_{GS}=±12V, V_{DS} =0V			±100	nA
Static Drain-source On Resistance	$R_{DS(ON)}$	V_{GS}=4.5V, I_D=20A		2.2	3.3	mΩ
		V_{GS}=2.5V, I_D=15A		2.9	4.5	mΩ
Forward Transconductance	g_{FS}	V_{DS} =10V, I_D=20A		25		S
Source-drain voltage	V_{SD}	Is=20A		0.80	1.00	V

●Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Input capacitance	C_{iss}	V_{DD} =10V f = 1MHz V_{GS} = 0V	-	5670	-	pF
Output capacitance	C_{oss}		-	460	-	
Reverse transfer capacitance	C_{rss}		-	416	-	

●Gate Charge characteristics(Tj=25℃,unless otherwise notse)

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Total gate charge	Q_g	V_{DD} =10V I_D = 15A V_{GS} = 4.5V	-	70.0	-	nC
Gate - Source charge	Q_{gs}		-	10.0	-	
Gate - Drain charge	Q_{gd}		-	14.0	-	

Note:

① Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2% ;

② Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate；

Fig.1 Gate-Charge Characteristics

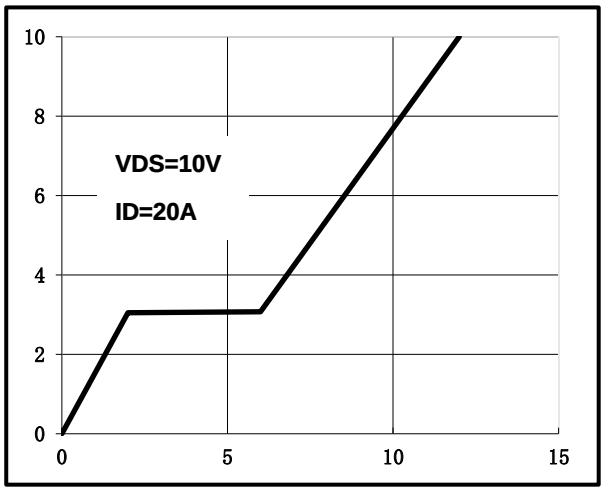


Fig.2 Capacitance Characteristics

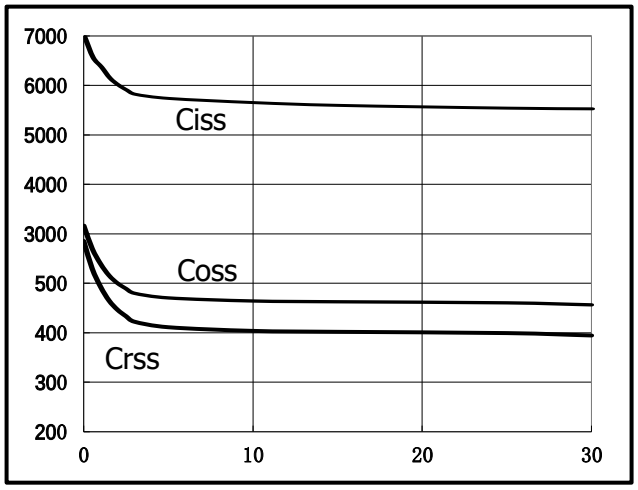


Fig.3 Power Dissipation Derating Curve

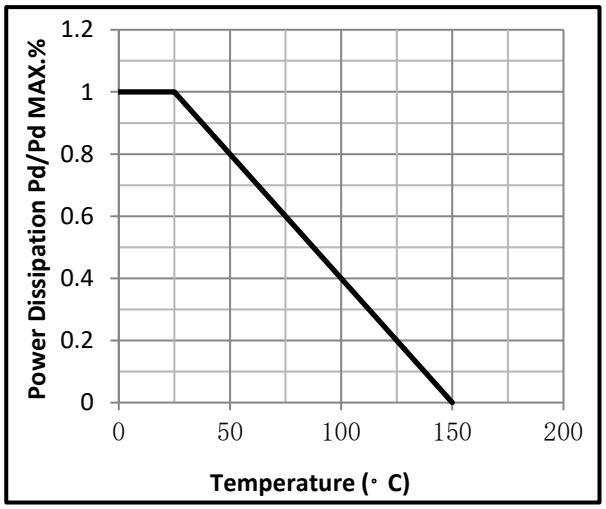


Fig.4 Typical output Characteristics

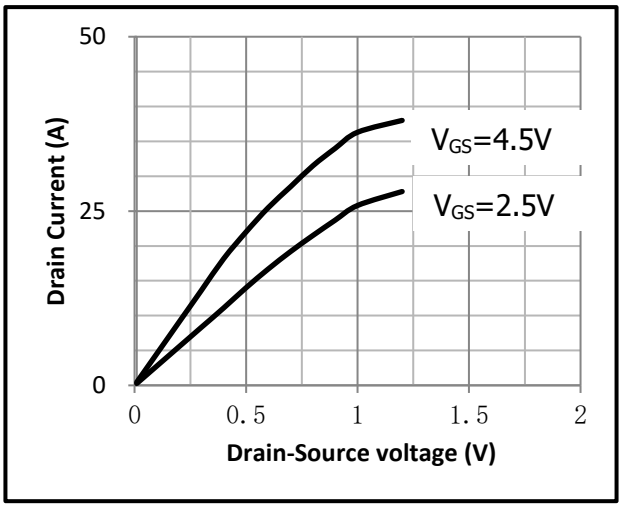


Fig.5 Threshold Voltage V.S Junction Temperature

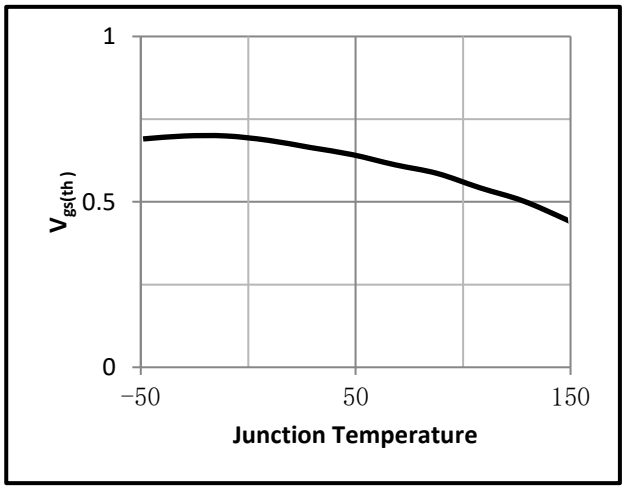


Fig.6 Resistance V.S Drain Current

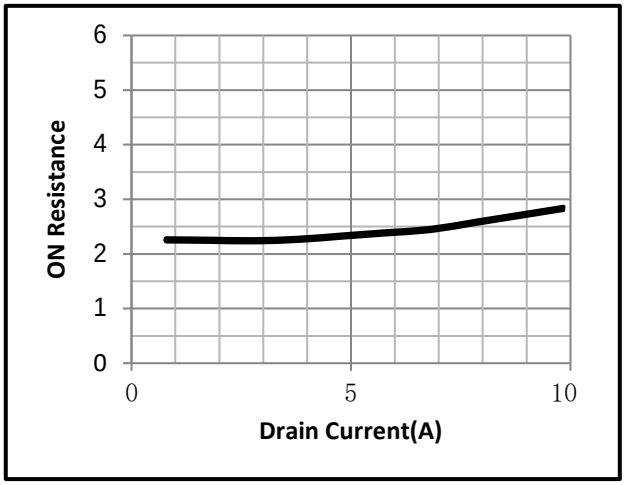


Fig.7 On-Resistance VS Gate Source Voltage

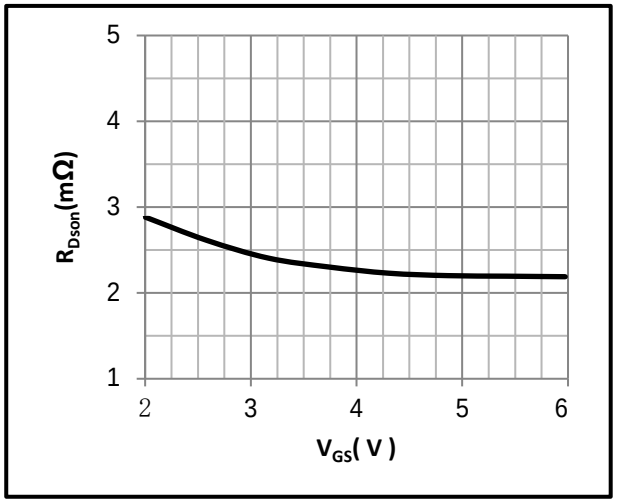


Fig.8 On-Resistance V.S Junction Temperature

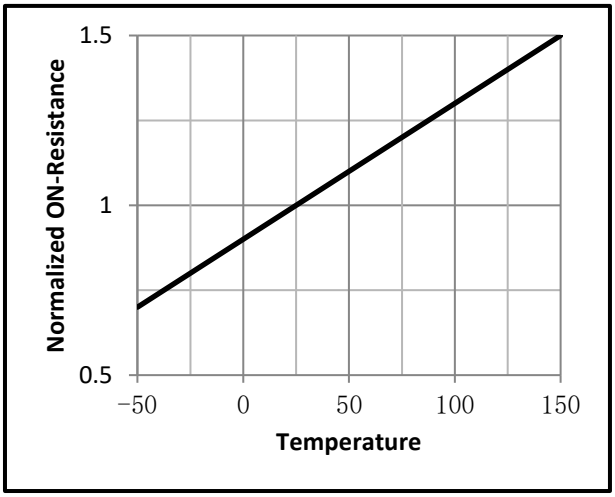


Fig.9 Switching Time Measurement Circuit

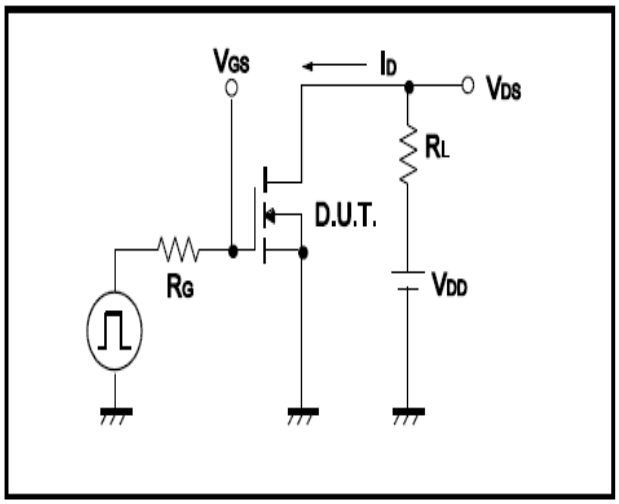


Fig.10 Gate Charge Waveform

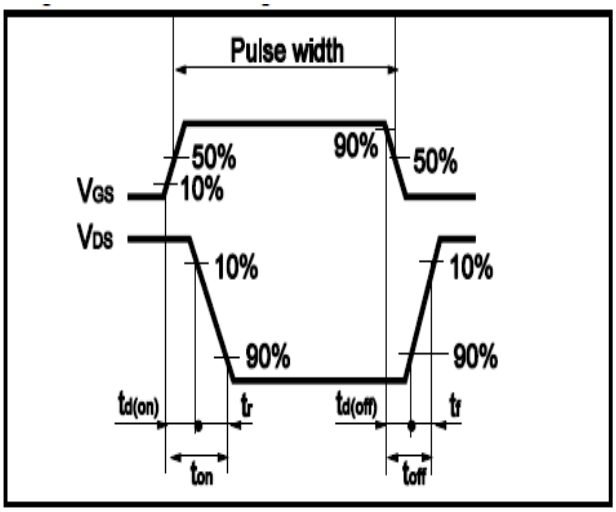


Fig.11 Avalanche Measurement Circuit

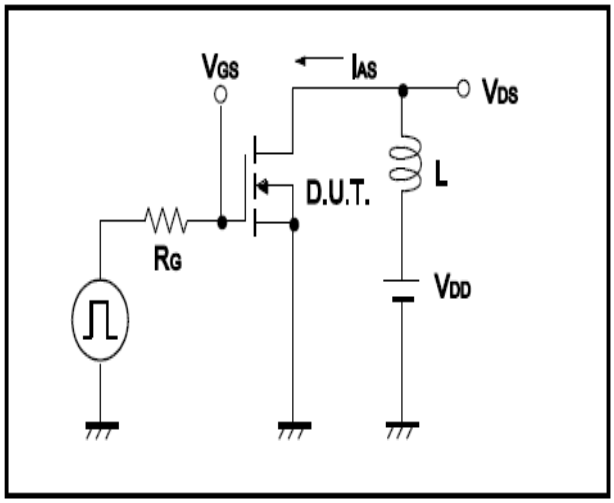
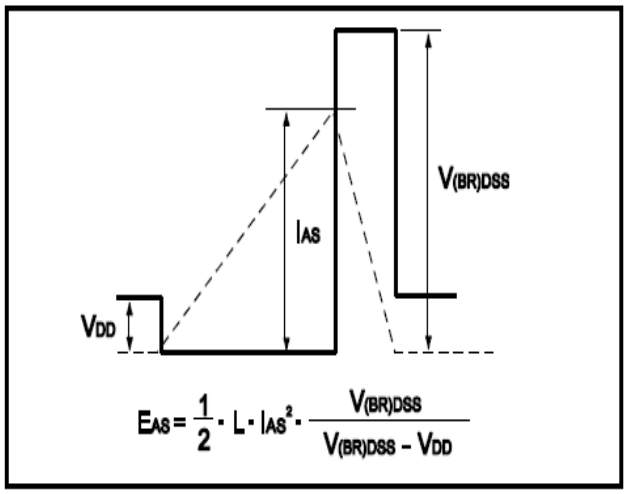
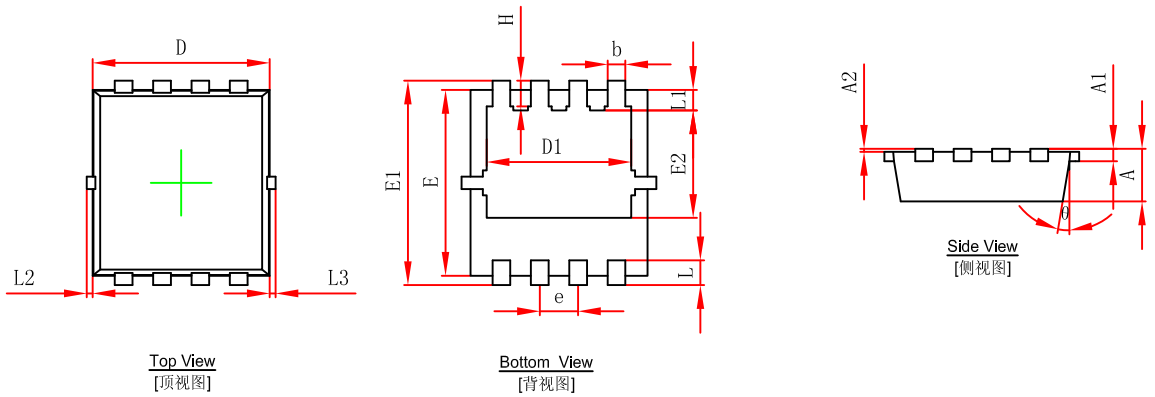


Fig.12 Avalanche Waveform

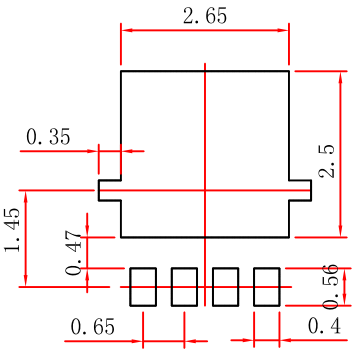


PDFN3333-8L Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.650	0.850	0.026	0.033
A1	0.152 REF.		0.006 REF.	
A2	0~0.05		0~0.002	
D	2.900	3.100	0.114	0.122
D1	2.300	2.600	0.091	0.102
E	2.900	3.100	0.114	0.122
E1	3.150	3.450	0.124	0.136
E2	1.535	1.935	0.060	0.076
b	0.200	0.400	0.008	0.016
e	0.550	0.750	0.022	0.030
L	0.300	0.500	0.012	0.020
L1	0.180	0.480	0.007	0.019
L2	0~0.100		0~0.004	
L3	0~0.100		0~0.004	
H	0.315	0.515	0.012	0.020
θ	9°	13°	9°	13°

PDFN3333-8L Suggested Pad Layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.05mm.
3.The pad layout is for reference purposes only.